

FEATURES

- Ultralow input noise at maximum gain:**
0.80 nV/ $\sqrt{\text{Hz}}$, 3.0 pA/ $\sqrt{\text{Hz}}$
- Two independent linear-in-dB channels**
- Absolute gain range per channel programmable:**
0 dB to 48 dB (preamp gain = 14 dB)
through 6 dB to 54 dB (preamp gain = 20 dB)
- ± 1.0 dB gain accuracy**
- Bandwidth: 40 MHz (-3 dB)**
- 300 k Ω input resistance**
- Variable gain scaling: 20 dB/V through 40 dB/V**
- Stable gain with temperature and supply variations**
- Single-ended unipolar gain control**
- Power shutdown at lower end of gain control**
- Drive ADCs directly**

APPLICATIONS

- Ultrasound and sonar time gain control**
- High performance AGC systems**
- Signal measurement**

GENERAL DESCRIPTION

The AD604 is an ultralow noise, very accurate, dual-channel, linear-in-dB variable gain amplifier (VGA) optimized for time-based variable gain control in ultrasound applications; however, it supports any application requiring low noise, wide bandwidth, variable gain control. Each channel of the AD604 provides a 300 k Ω input resistance and unipolar gain control for ease of use. User determined gain ranges, gain scaling (dB/V), and dc level shifting of output further optimize performance.

Each channel of the AD604 utilizes a high performance preamplifier that provides an input referred noise voltage of 0.8 nV/ $\sqrt{\text{Hz}}$. The very accurate linear-in-dB response of the AD604 is achieved with the differential input exponential amplifier (DSX-AMP) architecture. Each of the DSX-AMPs comprise a variable attenuator of 0 dB to 48.36 dB followed by a high speed fixed gain amplifier. The attenuator is a 7-stage R-1.5R ladder network. The attenuation between tap points is 6.908 dB and 48.36 dB for the ladder network.

The equation for the linear-in-dB gain response is

$$G(\text{dB}) = (\text{Gain Scaling (dB/V)} \times \text{VGN (V)}) + (\text{Preamp Gain (dB)} - 19 \text{ dB})$$

FUNCTIONAL BLOCK DIAGRAM

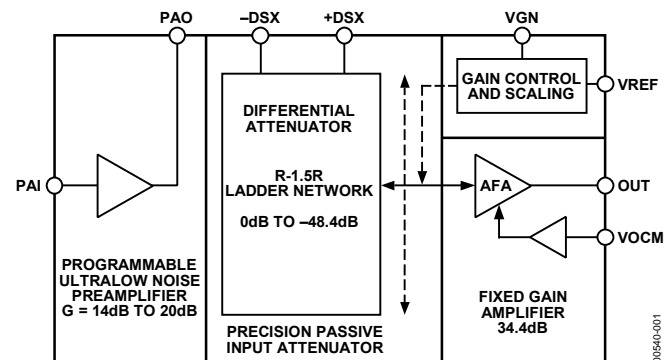


Figure 1.

Preamplifier gains between 5 and 10 (14 dB and 20 dB) provide overall gain ranges per channel of 0 dB through 48 dB and 6 dB through 54 dB. The two channels of the AD604 can be cascaded to provide greater levels of gain range by bypassing the second channel's preamplifier. However, in multiple channel systems, cascading the AD604 with other devices in the AD60x VGA family that do not include a preamplifier may provide a more efficient solution. The AD604 provides access to the output of the preamplifier, allowing for external filtering between the preamplifier and the differential attenuator stage.

Note that scale factors up to 40 dB/V are achievable with reduced accuracy for scales above 30 dB/V. The gain scales linearly-in-dB with control voltages of 0.4 V to 2.4 V with the 20 dB/V scale. Below and above this gain control range, the gain begins to deviate from the ideal linear-in-dB control law. The gain control region below 0.1 V is not used for gain control. In fact when the gain control voltage is <50 mV, the amplifier channel is powered down to 1.9 mA.

The AD604 is available in 24-lead SSOP, SOIC, and PDIP packages and is guaranteed for operation over the -40°C to $+85^{\circ}\text{C}$ temperature range.

Rev. C

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TABLE OF CONTENTS

Features	1	Applications Information	18
Applications	1	An Ultralow Noise AGC Amplifier with 82 dB to 96 dB	
Functional Block Diagram	1	Gain Range	19
General Description	1	Ultralow Noise, Differential Input-Differential	
Revision History	2	Output VGA	21
Specifications	3	Medical Ultrasound TGC Driving the AD9050, a 10-Bit,	
Absolute Maximum Ratings	5	40 MSPS ADC	22
ESD Caution	5	Evaluation Board	24
Pin Configuration and Function Descriptions	6	Using the Preamp	24
Typical Performance Characteristics	7	DSX Input Connections	24
Theory of Operation	13	Preamplifier Gain	25
Preamplifier	14	Outputs	25
Differential Ladder (Attenuator)	15	DC Operating Conditions	25
AC Coupling	16	Evaluation Board Artwork and Schematic	26
Gain Control Interface	16	Outline Dimensions	28
Active Feedback Amplifier (Fixed Gain Amp)	16	Ordering Guide	29

REVISION HISTORY

3/07—Rev. B to Rev. C

Added Evaluation Board section	24
Added Evaluation Board Artwork and Schematics Section	26
Changes to Ordering Guide	29

12/06—Rev. A to Rev. B

Changes to General Description	1
Changes to Figure 54	23
Changes to Ordering Guide	25

1/04—Rev. 0 to Rev. A

Changes to Specifications	2
Changes to Absolute Maximum Ratings	3
Changes to Ordering Guide	3
Changes to Figure 1 Caption	5
Changes to Figure 11 Caption	6
Changes to Figure 17	6
Changes to Figure 51	17
Updated Outline Dimensions	18

10/96—Revision 0: Initial Version

SPECIFICATIONS

Each amplifier channel at $T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{ V}$, $R_S = 50\ \Omega$, $R_L = 500\ \Omega$, $C_L = 5\ \text{pF}$, $V_{\text{REF}} = 2.50\ \text{V}$ (scaling = 20 dB/V), 0 dB to 48 dB gain range (preamplifier gain = 14 dB), $\text{VOCM} = 2.5\ \text{V}$, C_1 and $C_2 = 0.1\ \mu\text{F}$ (see Figure 37), unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Preamplifier					
Input Resistance			300		k Ω
Input Capacitance			8.5		pF
Input Bias Current			-27		mA
Peak Input Voltage	Preamp gain = 14 dB		± 400		mV
	Preamp gain = 20 dB		± 200		mV
Input Voltage Noise	VGN = 2.9 V, $R_S = 0\ \Omega$				
	Preamp gain = 14 dB		0.8		nV/ $\sqrt{\text{Hz}}$
	Preamp gain = 20 dB		0.73		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	Independent of gain		3.0		pA/ $\sqrt{\text{Hz}}$
Noise Figure	$R_S = 50\ \Omega$, $f = 10\ \text{MHz}$, VGN = 2.9 V		2.3		dB
	$R_S = 200\ \Omega$, $f = 10\ \text{MHz}$, VGN = 2.9 V		1.1		dB
DSX					
Input Resistance			175		Ω
Input Capacitance			3.0		pF
Peak Input Voltage			2.5 ± 2		V
Input Voltage Noise	VGN = 2.9 V		1.8		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	VGN = 2.9 V		2.7		pA/ $\sqrt{\text{Hz}}$
Noise Figure	$R_S = 50\ \Omega$, $f = 10\ \text{MHz}$, VGN = 2.9 V		8.4		dB
	$R_S = 200\ \Omega$, $f = 10\ \text{MHz}$, VGN = 2.9 V		12		dB
Common-Mode Rejection Ratio	$f = 1\ \text{MHz}$, VGN = 2.65 V		-20		dB
OUTPUT CHARACTERISTICS					
-3 dB Bandwidth	Constant with gain		40		MHz
Slew Rate	VGN = 1.5 V, output = 1 V step		170		V/ μs
Output Signal Range	$R_L \geq 500\ \Omega$		2.5 ± 1.5		V
Output Impedance	$f = 10\ \text{MHz}$		2		Ω
Output Short-Circuit Current			± 40		mA
Harmonic Distortion					
	VGN = 1 V, $V_{\text{OUT}} = 1\ \text{V p-p}$				
HD2	$f = 1\ \text{MHz}$		-54		dBc
HD3	$f = 1\ \text{MHz}$		-67		dBc
HD2	$f = 10\ \text{MHz}$		-43		dBc
HD3	$f = 10\ \text{MHz}$		-48		dBc
Two-Tone Intermodulation					
	VGN = 2.9 V, $V_{\text{OUT}} = 1\ \text{V p-p}$				
Distortion (IMD)	$f = 1\ \text{MHz}$		-74		dBc
	$f = 10\ \text{MHz}$		-71		dBc
Third-Order Intercept					
	$f = 10\ \text{MHz}$, VGN = 2.65 V, $V_{\text{OUT}} = 1\ \text{V p-p}$, input referred		-12.5		dBm
1 dB Compression Point	$f = 1\ \text{MHz}$, VGN = 2.9 V, output referred		15		dBm
Channel-to-Channel Crosstalk	$V_{\text{OUT}} = 1\ \text{V p-p}$, $f = 1\ \text{MHz}$, Channel 1: VGN = 2.65 V, inputs shorted, Channel 2: VGN = 1.5 V (mid gain)		-30		dB
Group Delay Variation	$1\ \text{MHz} < f < 10\ \text{MHz}$, full gain range		± 2		ns
VOCM Input Resistance			45		k Ω

AD604

Parameter	Conditions	Min	Typ	Max	Unit
ACCURACY					
Absolute Gain Error					
0 dB to 3 dB	0.25 V < VGN < 0.400 V	-1.2	+0.75	+3	dB
3 dB to 43 dB	0.400 V < VGN < 2.400 V	-1.0	±0.3	+1.0	dB
43 dB to 48 dB	2.400 V < VGN < 2.65 V	-3.5	-1.25	+1.2	dB
Gain Scaling Error	0.400 V < VGN < 2.400 V		±0.25		dB/V
Output Offset Voltage	VREF = 2.500 V, VOVM = 2.500 V	-50	±30	+50	mV
Output Offset Variation	VREF = 2.500 V, VOVM = 2.500 V		30	50	mV
GAIN CONTROL INTERFACE					
Gain Scaling Factor	VREF = 2.5 V, 0.4 V < VGN < 2.4 V VREF = 1.67 V	19	20 30	21	dB/V dB/V
Gain Range	Preamp gain = 14 dB Preamp gain = 20 dB		0 to 48 6 to 54		dB dB
Input Voltage (VGN) Range	20 dB/V, VREF = 2.5 V		0.1 to 2.9		V
Input Bias Current			-0.4		µA
Input Resistance			2		MΩ
Response Time	48 dB gain change		0.2		µs
VREF Input Resistance			10		kΩ
POWER SUPPLY					
Specified Operating Range	One complete channel One DSX only		±5 5		V V
Power Dissipation	One complete channel One DSX only		220 95		mW mW
Quiescent Supply Current	VPOS, one complete channel VPOS, one DSX only VNEG, one preamplifier only		32 19 -15	36 23	mA mA mA
Powered Down	VPOS, VGN < 50 mV, one channel VNEG, VGN < 50 mV, one channel		1.9 -150	3.0	mA µA
Power-Up Response Time	48 dB gain change, V _{OUT} = 2 V p-p		0.6		µs
Power-Down Response Time			0.4		µs

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter ^{1, 2}	Rating
Supply Voltage $\pm V_S$	
Pins[17:20] (with Pin 16, Pin 22 = 0 V)	± 6.5 V
Input Voltages	
Pin 1, Pin 2, Pin 11, Pin 12	$V_{POS}/2 \pm 2$ V Continuous
Pin 4, Pin 9	± 2 V
Pin 5, Pin 8	V_{POS}, V_{NEG}
Pin 6, Pin 7, Pin 13, Pin 14, Pin 23, Pin 24	$V_{POS}, 0$ V
Internal Power Dissipation	
PDIP (N)	2.2 W
SOIC (RW)	1.7 W
SSOP (RS)	1.1 W
Operating Temperature Range	-40°C to $+85^{\circ}\text{C}$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature, Soldering 60 sec	300°C
θ_{JA} ³	
AD604AN	$105^{\circ}\text{C}/\text{W}$
AD604AR	$73^{\circ}\text{C}/\text{W}$
AD604ARS	$112^{\circ}\text{C}/\text{W}$
θ_{JC} ³	
AD604AN	$35^{\circ}\text{C}/\text{W}$
AD604AR	$38^{\circ}\text{C}/\text{W}$
AD604ARS	$34^{\circ}\text{C}/\text{W}$

¹ Pins 1, 2, 11, 12, 13, 14, 23, and 24 are part of a single-supply circuit. The part is likely to suffer damaged if any of these pins are accidentally connected to VN.

² When driven from an external low impedance source.

³ Using MIL-STD-883 test method G43-87 with a 1S (2-layer) test board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

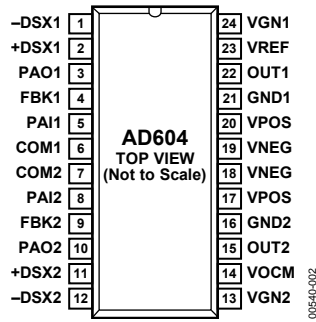


Figure 2.

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	-DSX1	CH1 Negative Signal Input to DSX1.
2	+DSX1	CH1 Positive Signal Input to DSX1.
3	PAO1	CH1 Preamplifier Output.
4	FBK1	CH1 Preamplifier Feedback Pin.
5	PAI1	CH1 Preamplifier Positive Input.
6	COM1	CH1 Signal Ground. When connected to positive supply, Preamplifier 1 shuts down.
7	COM2	CH2 Signal Ground. When connected to positive supply, Preamplifier 2 shuts down.
8	PAI2	CH2 Preamplifier Positive Input.
9	FBK2	CH2 Preamplifier Feedback Pin.
10	PAO2	CH2 Preamplifier Output.
11	+DSX2	CH2 Positive Signal Input to DSX2.
12	-DSX2	CH2 Negative Signal Input to DSX2.
13	VGN2	CH2 Gain-Control Input and Power-Down Pin. If grounded, device is off; otherwise, positive voltage increases gain.
14	VOCM	Input to this pin defines the common-mode of the output at OUT1 and OUT2.
15	OUT2	CH2 Signal Output.
16	GND2	Ground.
17	VPOS	Positive Supply.
18	VNEG	Negative Supply.
19	VNEG	Negative Supply.
20	VPOS	Positive Supply.
21	GND1	Ground.
22	OUT1	CH1 Signal Output.
23	VREF	Input to this pin sets gain-scaling for both channels to 2.5 V = 20 dB/V, 1.67 V = 30 dB/V.
24	VGN1	CH1 Gain-Control Input and Power-Down Pin. If grounded, the device is off; otherwise, positive voltage increases gain.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, G (preamp) = 14 dB, VREF = 2.5 V (20 dB/V scaling), f = 1 MHz, RL = 500 Ω, CL = 5 pF, TA = 25°C, and VSS = ±5 V.

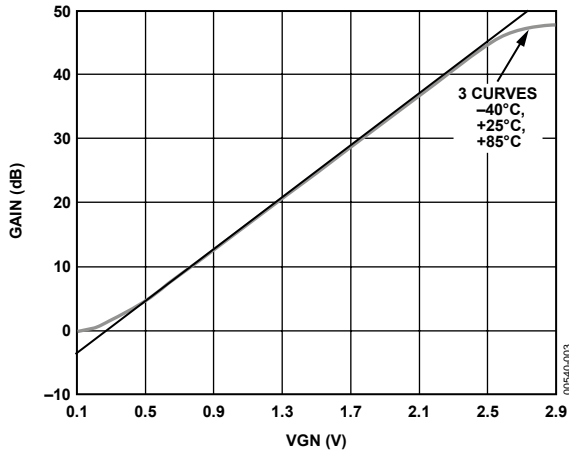


Figure 3. Gain vs. VGN for Three Temperatures

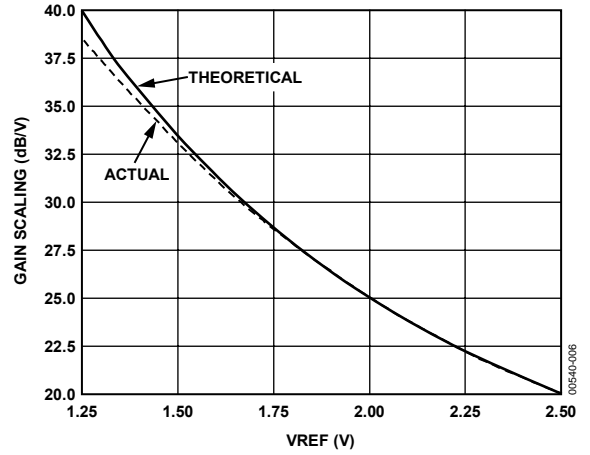


Figure 6. Gain Scaling vs. VREF

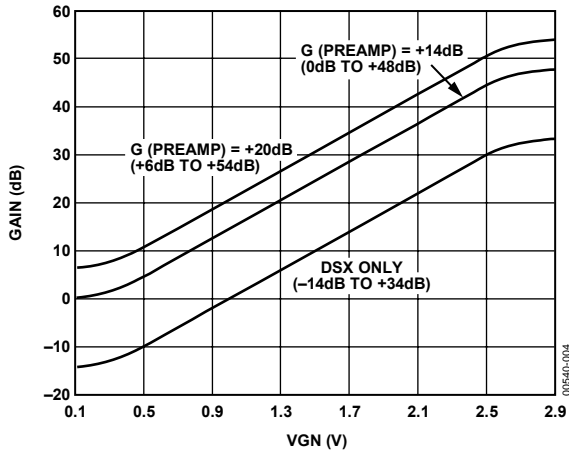


Figure 4. Gain vs. VGN for Different Preamp Gains

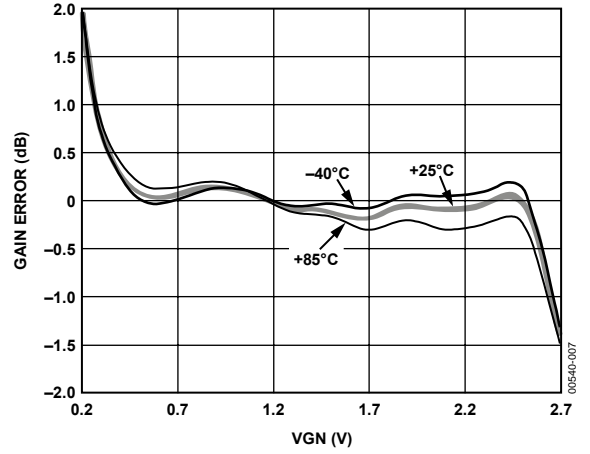


Figure 7. Gain Error vs. VGN

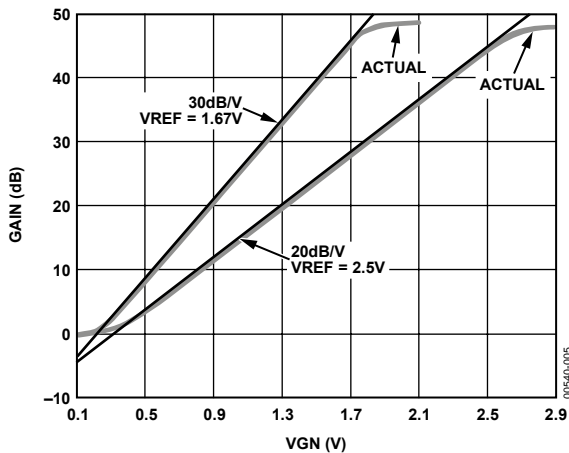


Figure 5. Gain vs. VGN for Different Gain Scalings

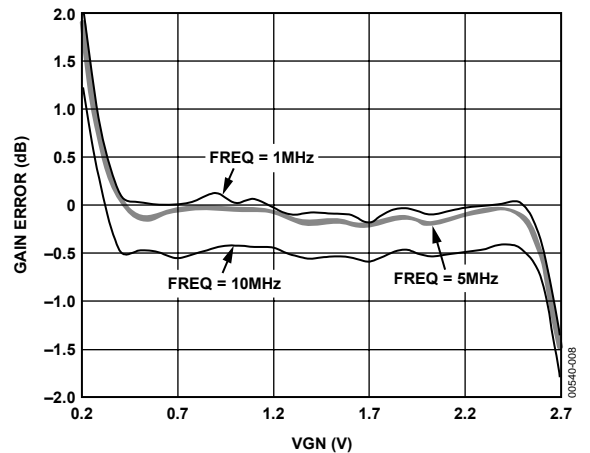


Figure 8. Gain Error vs. VGN at Different Frequencies

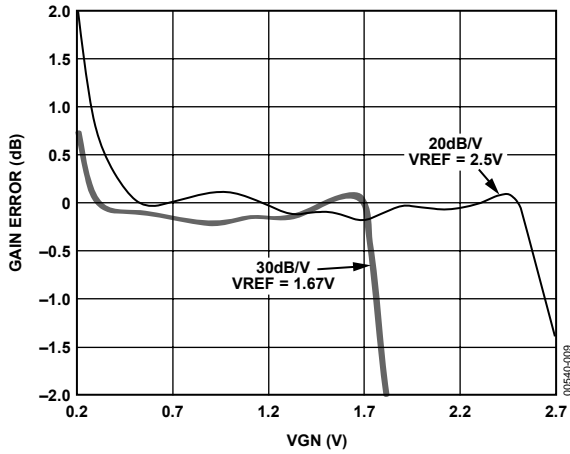


Figure 9. Gain Error vs. VGN for Two Gain Scaling Values

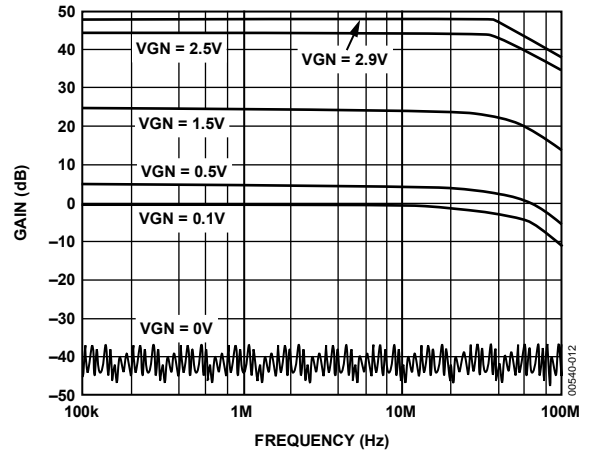


Figure 12. AC Response for Various Values of VGN

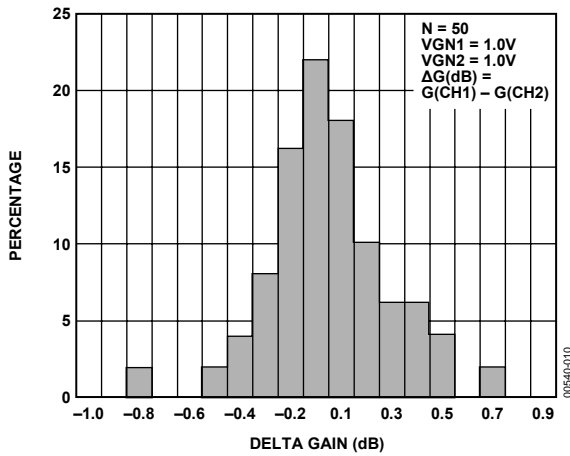


Figure 10. Gain Match; VGN1 = VGN2 = 1.0V

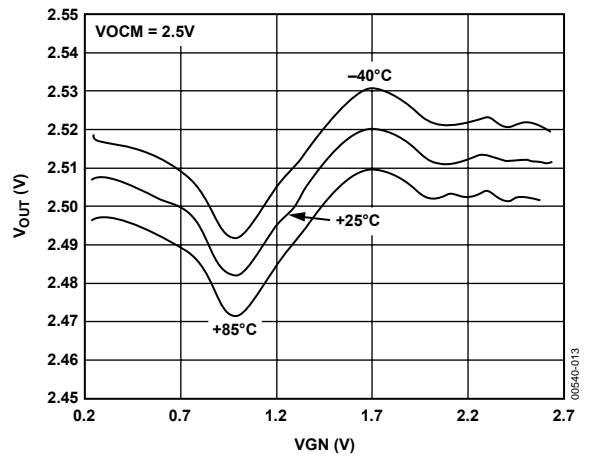


Figure 13. Output Offset vs. VGN for Three Temperatures

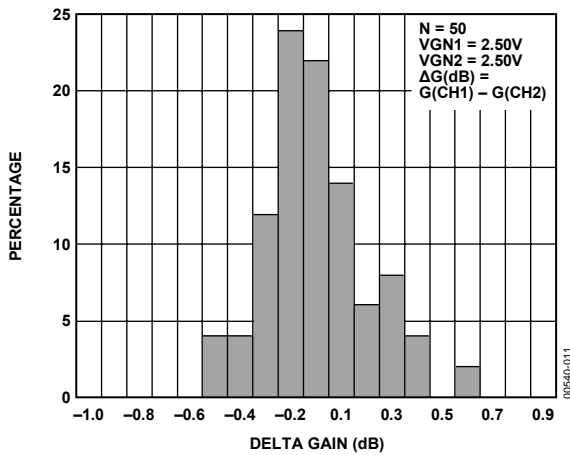


Figure 11. Gain Match; VGN1 = VGN2 = 2.50V

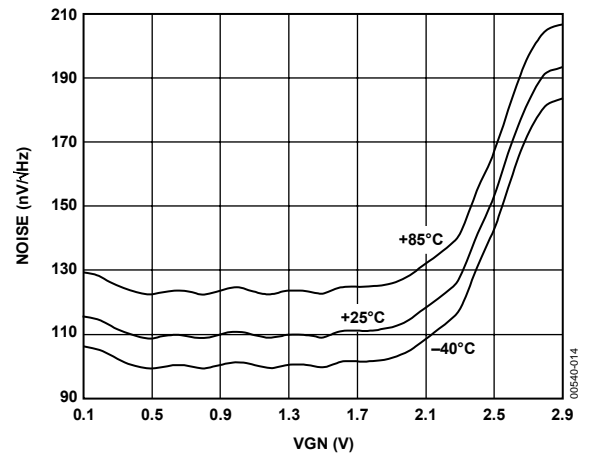


Figure 14. Output Referred Noise vs. VGN for Three Temperatures

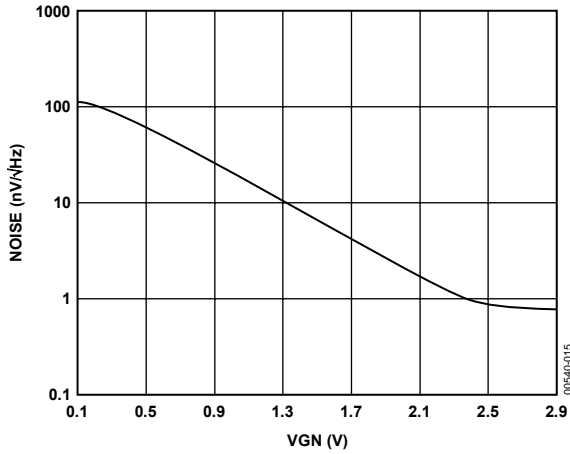


Figure 15. Input Referred Noise vs. VGN

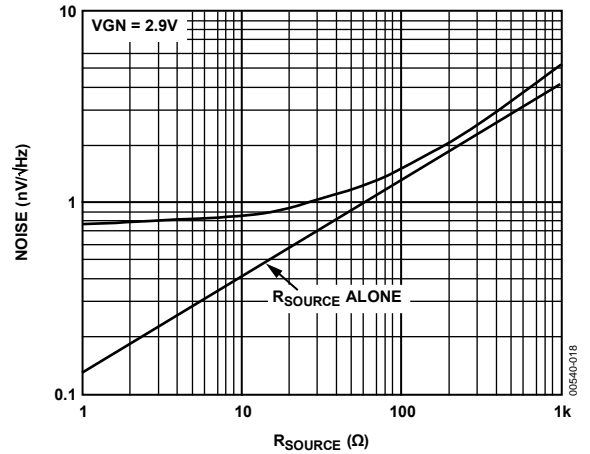


Figure 18. Input Referred Noise vs. R_{SOURCE}

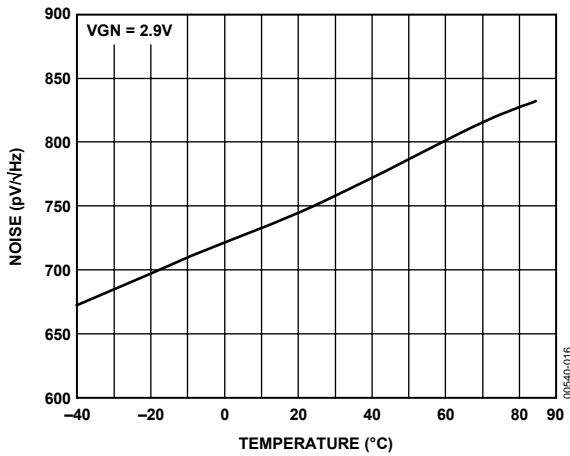


Figure 16. Input Referred Noise vs. Temperature

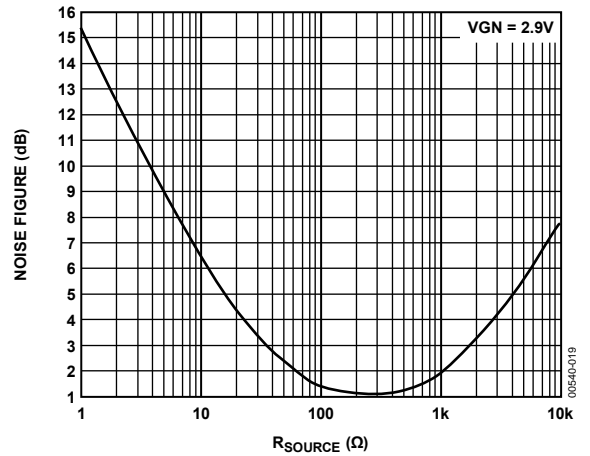


Figure 19. Noise Figure vs. R_{SOURCE}

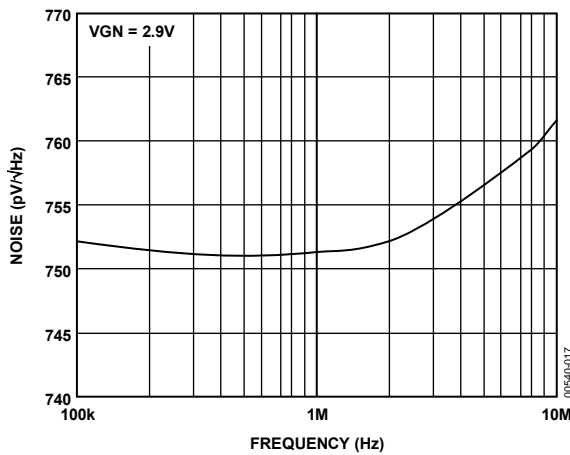


Figure 17. Input Referred Noise vs. Frequency

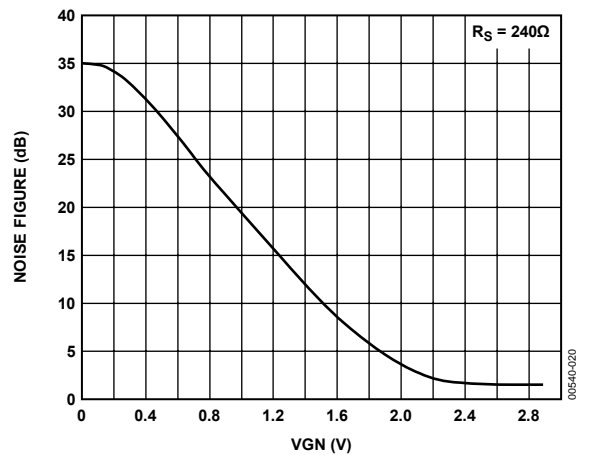


Figure 20. Noise Figure vs. VGN

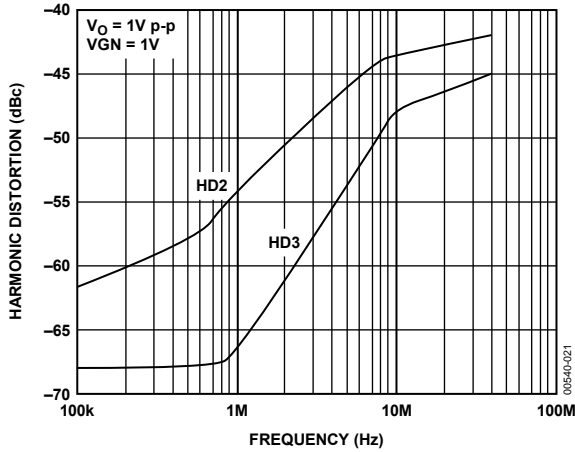


Figure 21. Harmonic Distortion vs. Frequency

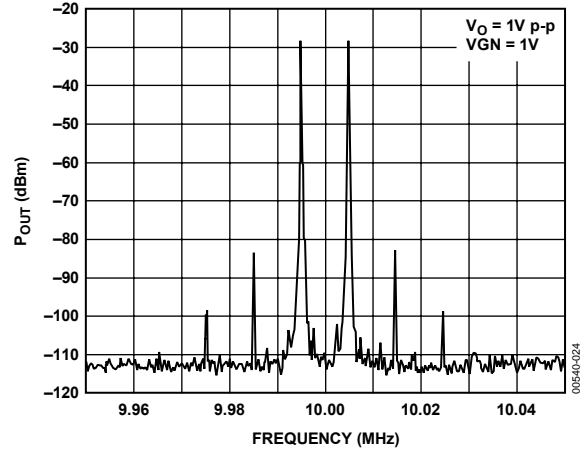


Figure 24. Intermodulation Distortion

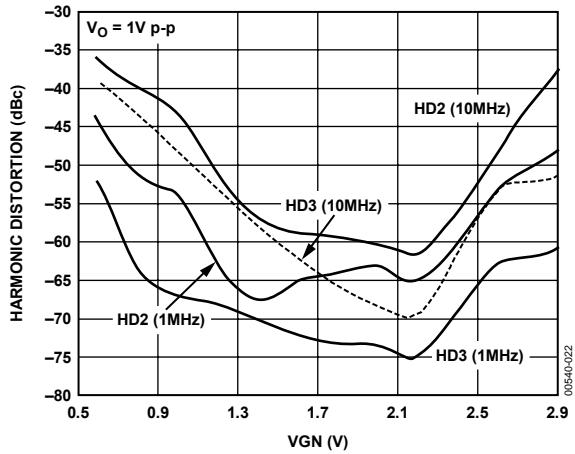


Figure 22. Harmonic Distortion vs. VGN

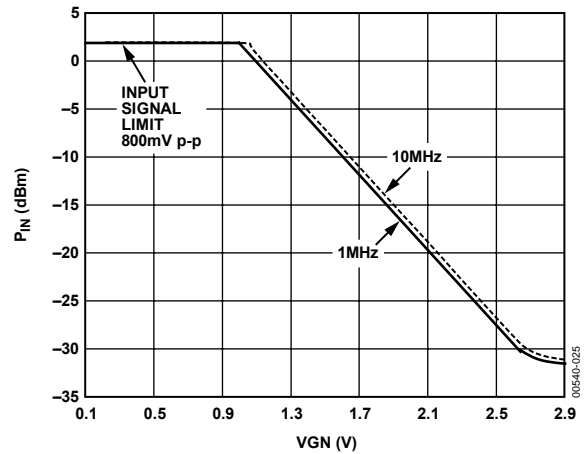


Figure 25. 1 dB Compression vs. VGN

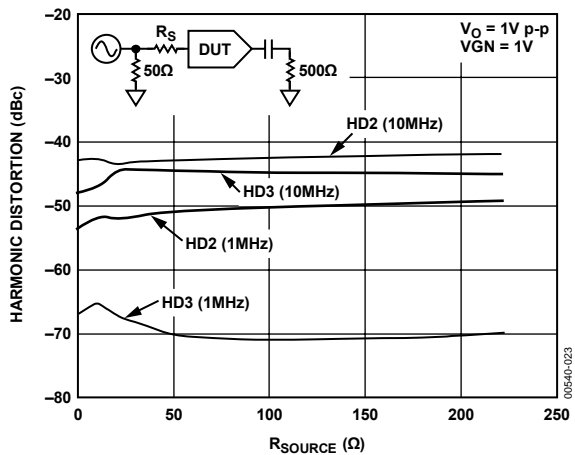


Figure 23. Harmonic Distortion vs. R_{SOURCE}

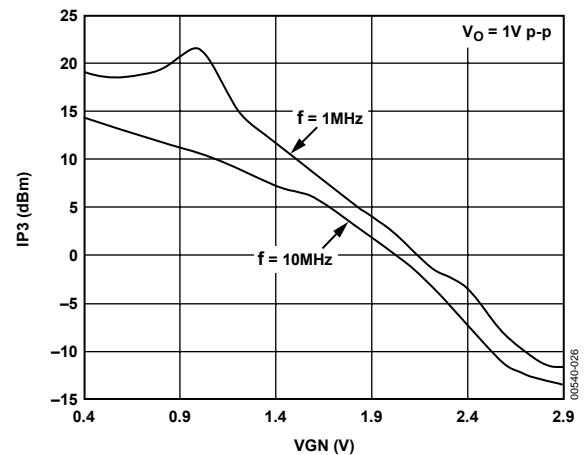


Figure 26. Third-Order Intercept vs. VGN

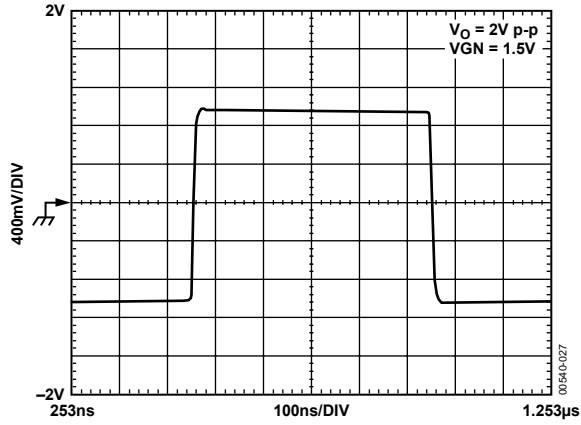


Figure 27. Large Signal Pulse Response

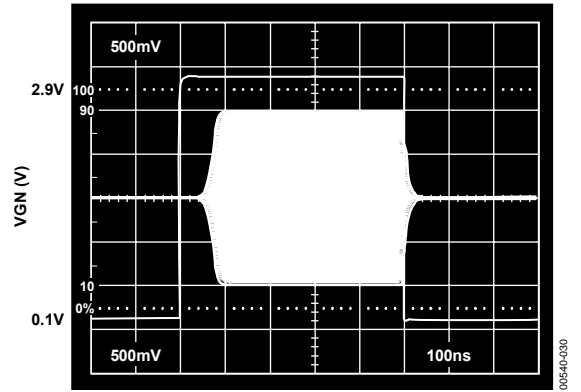


Figure 30. Gain Response

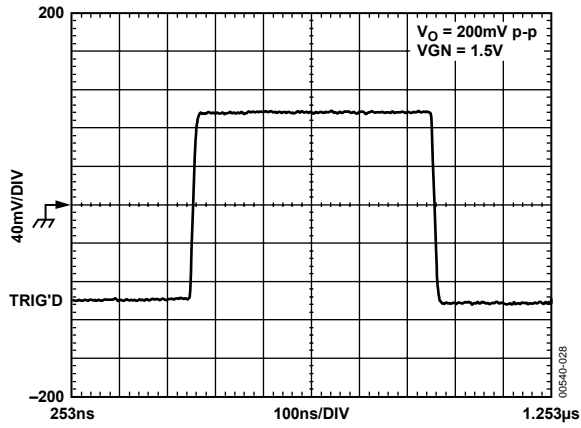


Figure 28. Small Signal Pulse Response

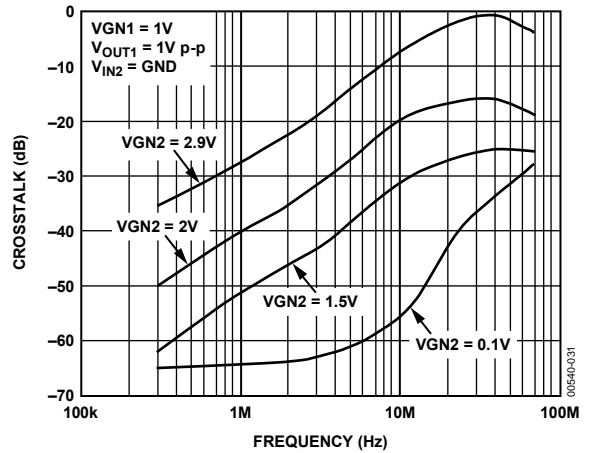


Figure 31. Crosstalk (CH1 to CH2) vs. Frequency

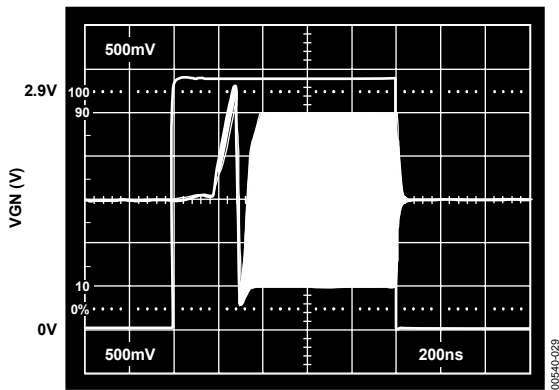


Figure 29. Power-Up/Power-Down Response

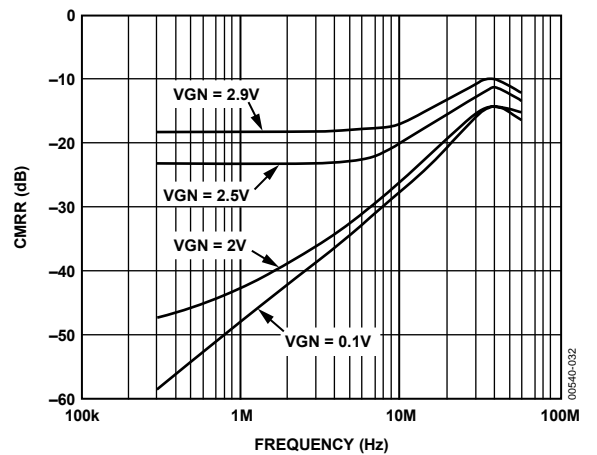


Figure 32. DSX Common-Mode Rejection Ratio vs. Frequency

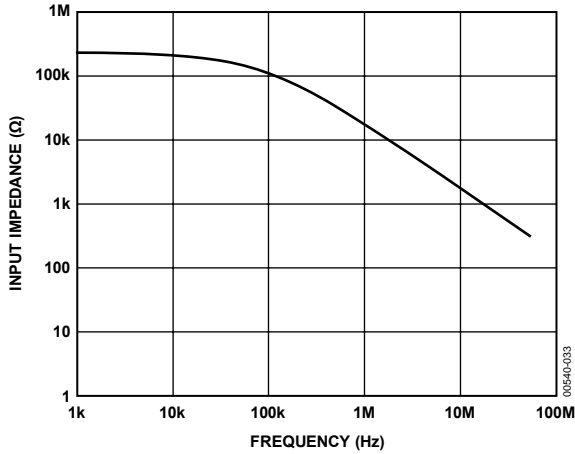


Figure 33. Input Impedance vs. Frequency

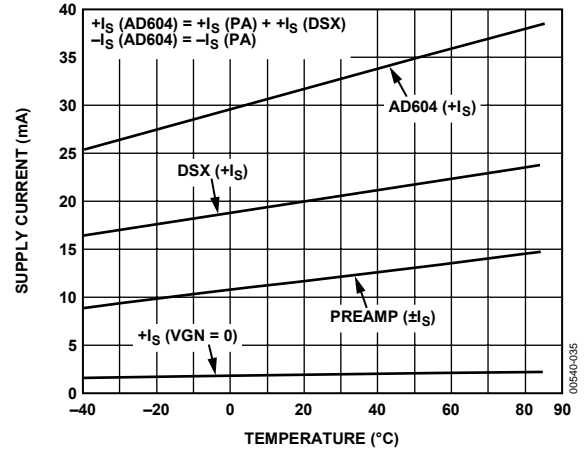


Figure 35. Supply Current (One Channel) vs. Temperature

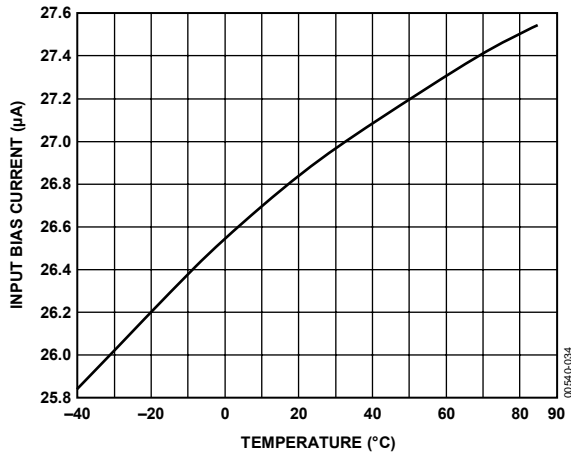


Figure 34. Input Bias Current vs. Temperature

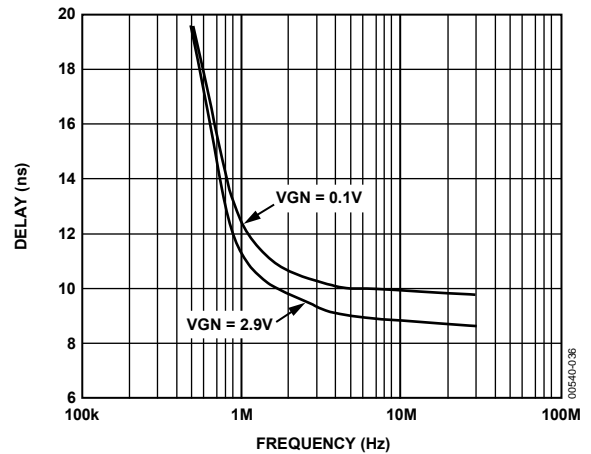


Figure 36. Group Delay vs. Frequency

THEORY OF OPERATION

The AD604 is a dual-channel, variable gain amplifier with an ultralow noise preamplifier. Figure 37 shows the simplified block diagram of one channel. Each identical channel consists of:

1. A preamplifier with gain setting resistors (R5, R6, and R7).
2. A single-supply X-AMP® (hereafter called DSX, differential single-supply X-AMP), made up of:
 - A precision passive attenuator (differential ladder).
 - A gain control block.
 - A VOCM buffer with supply splitting resistors (R3 and R4).
 - An active feedback amplifier (AFA) with gain setting resistors (R1 and R2). (To understand the active-feedback amplifier topology, refer to the AD830 data sheet. The AD830 is a practical implementation of the idea.)

The preamplifier is powered by a ± 5 V supply, while the DSX uses a single +5 V supply. The linear-in-dB gain response of the AD604 can generally be described by

$$G \text{ (dB)} = \text{Gain Scaling (dB/V)} \times \text{Gain Control (V)} + (\text{Preamp Gain (dB)} - 19 \text{ dB}) \quad (1)$$

Each channel provides between 0 dB to 48.4 dB through 6 dB to 54.4 dB of gain, depending on the user determined preamplifier gain. The center 40 dB of gain is exactly linear-in-dB while the gain error increases at the top and bottom of the range. The gain of the preamplifier is typically either 14 dB or 20 dB but can be set to intermediate values by a single external resistor (see the Preamplifier section for details). The gain of the DSX can vary from -14 dB to $+34.4$ dB, as is determined by the gain control voltage (VGN). The VREF input establishes the gain scaling; the

useful gain scaling range is between 20 dB/V and 40 dB/V for a VREF voltage of 2.5 V and 1.25 V, respectively. For example, if the preamp gain was set to 14 dB and VREF was set to 2.50 V (to establish a gain scaling of 20 dB/V), the gain equation would simplify to

$$G \text{ (dB)} = 20 \text{ (dB/V)} \times \text{VGN (V)} - 5 \text{ dB}$$

The desired gain can then be achieved by setting the unipolar gain control (VGN) to a voltage within its nominal operating range of 0.25 V to 2.65 V (for 20 dB/V gain scaling). The gain is monotonic for a complete gain control voltage range of 0.1 V to 2.9 V. Maximum gain can be achieved at a VGN of 2.9 V.

The inputs VREF and VOCM are common to both channels. They are decoupled to ground, minimizing inter-channel crosstalk. For highest gain scaling accuracy, VREF should have an external low impedance voltage source. For low accuracy 20 dB/V applications, the VREF input can be decoupled with a capacitor to ground. In this mode, the gain scaling is determined by the midpoint between VPOS and GND, so care should be taken to control the supply voltage to 5 V. The input resistance looking into the VREF pin is $10 \text{ k}\Omega \pm 20\%$.

The DSX portion of the AD604 is a single-supply circuit, and the VOCM pin is used to establish the dc level of the midpoint of this portion of the circuit. VOCM needs only an external decoupling capacitor to ground to center the midpoint between the supply voltages (5 V, GND); however, if the dc level of the output is important to the user (see the Applications Information section for AD9050 example), then VOCM can be specifically set. The input resistance looking into the VOCM pin is $45 \text{ k}\Omega \pm 20\%$.

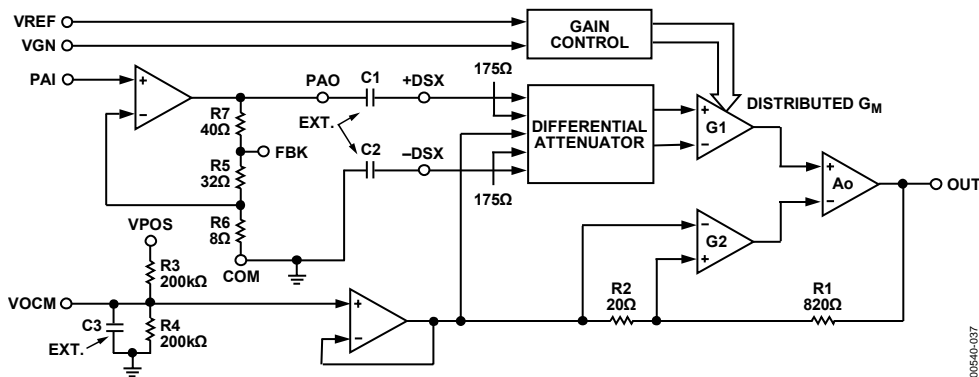


Figure 37. Simplified Block Diagram of a Single Channel of the AD604

PREAMPLIFIER

The input capability of the following single-supply DSX (2.5 ± 2 V for a +5 V supply) limits the maximum input voltage of the preamplifier to ± 400 mV for the 14 dB gain configuration or ± 200 mV for the 20 dB gain configuration.

The preamplifier gain can be programmed to 14 dB or 20 dB by either shorting the FBK1 node to PAO1 (14 dB) or by leaving Node FBK1 open (20 dB). These two gain settings are very accurate since they are set by the ratio of on-chip resistors. Any intermediate gain can be achieved by connecting the appropriate resistor value between PAO1 and FBK1 according to Equation 2 and Equation 3:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{(R7 \parallel R_{EXT}) + R5 + R6}{R6} \quad (2)$$

$$R_{EXT} = \frac{[R6 \times G - (R5 + R6)] \times R7}{R7 - (R6 \times G) + (R5 + R6)} \quad (3)$$

Since the internal resistors have an absolute tolerance of $\pm 20\%$, the gain can be in error by as much as 0.33 dB when R_{EXT} is 30Ω , where it was assumed that R_{EXT} is exact.

Figure 38 shows how the preamplifier is set to gains of 14 dB, 17.5 dB, and 20 dB. The gain range of a single channel of the AD604 is 0 dB to 48 dB when the preamplifier is set to 14 dB (Figure 38a), 3.5 dB to 51.5 dB for a preamp gain of 17.5 dB (Figure 38b), and 6 dB to 54 dB for the highest preamp gain of 20 dB (Figure 38c).

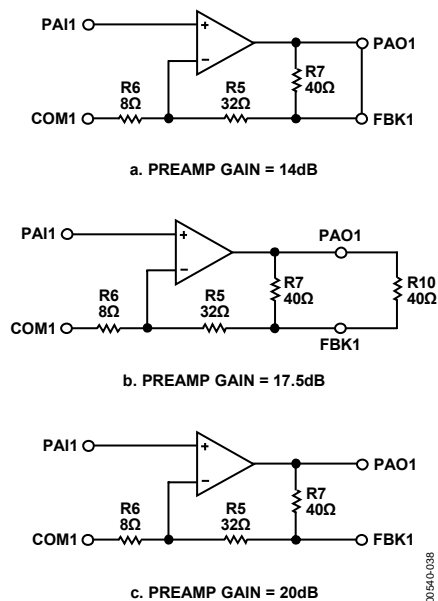


Figure 38. Preamplifier Gain Programmability

For a preamplifier gain of 14 dB, the preamplifier's -3 dB small signal bandwidth is 130 MHz. When the gain is at its maximum of 20 dB, the bandwidth is reduced by half to 65 MHz. Figure 39 shows the ac response for the three preamp gains shown in Figure 38. Note that the gain for an R_{EXT} of 40Ω should be 17.5 dB, but the mismatch between the internal resistors and the external resistor caused the actual gain for this particular

preamplifier to be 17.7 dB. The -3 dB small signal bandwidth of one complete channel of the AD604 (preamplifier and DSX) is 40 MHz and is independent of gain.

To achieve optimum specifications, power and ground management are critical to the AD604. Large dynamic currents result because of the low resistances needed for the desired noise performance. Most of the difficulty is with the very low gain setting resistors of the preamplifier that allow for a total input referred noise, including the DSX, as low as 0.8 nV/ $\sqrt{\text{Hz}}$. The consequently large dynamic currents have to be carefully handled to maintain performance even at large signal levels.

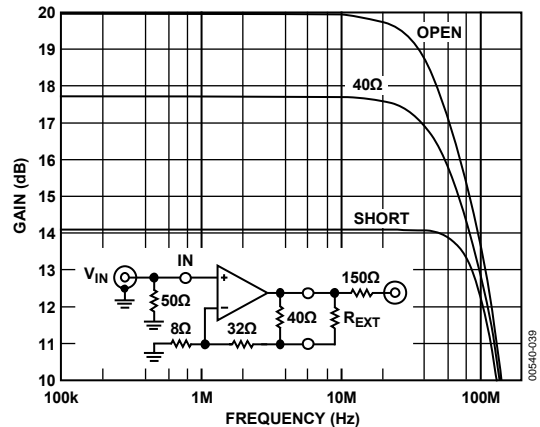


Figure 39. AC Response for Preamplifier Gains of 14 dB, 17.5 dB, and 20 dB

The preamplifier uses a dual ± 5 V supply to accommodate large dynamic currents and a ground referenced input. The preamp output is also ground referenced, and requires a common-mode level shift into the single-supply DSX. The two external coupling capacitors (C1 and C2 in Figure 37) connected to Nodes PAO1 and +DSX, and $-DSX$ and ground, respectively, perform this function (see the AC Coupling section). In addition, they eliminate any offset that would otherwise be introduced by the preamplifier. It should be noted that an offset of 1 mV at the input of the DSX is amplified by 34.4 dB ($\times 52.5$) when the gain control voltage is at its maximum; this equates to 52.5 mV at the output. AC coupling is consequently required to keep the offset from degrading the output signal range.

The gain-setting preamplifier feedback resistors are small enough (8Ω and 32Ω) that even an additional 1Ω in the ground connection at Pin COM1, (the input common-mode reference), seriously degrades gain accuracy and noise performance. This node is very sensitive and careful attention is necessary to minimize the ground impedance. All connections to node COM1 should be as short as possible.

The preamplifier, including the gain setting resistors, has a noise performance of 0.71 nV/ $\sqrt{\text{Hz}}$ and 3 pA/ $\sqrt{\text{Hz}}$. Note that a significant portion of the total input referred voltage noise is due to the feedback resistors. The equivalent noise resistance presented by $R5$ and $R6$ in parallel is nominally 6.4Ω , which contributes 0.33 nV/ $\sqrt{\text{Hz}}$ to the total input referred voltage noise. The larger portion of the input referred voltage noise is coming from the amplifier with 0.63 nV/ $\sqrt{\text{Hz}}$. The current noise

is independent of gain and depends only on the bias current in the input stage of the preamplifier—it is $3 \text{ pA}/\sqrt{\text{Hz}}$.

The preamplifier can drive 40Ω (the nominal feedback resistors) and the following 175Ω ladder load of the DSX with low distortion. For example, at 10 MHz and 1 V at the output, the preamplifier has less than -45 dB of second and third harmonic distortion when driven from a low (25Ω) source resistance.

In applications that require more than 48 dB of gain range, two AD604 channels may be cascaded. Since the preamplifier has a limited input signal range, consumes over half (120 mW) of the total power (220 mW), and its ultralow noise is not necessary after the first AD604 channel, a shutdown mechanism that disables only the preamplifier is provided. All that is required to shut down the preamplifier is to connect the COM1 and/or COM2 pin to the positive supply; the DSX is unaffected. For additional details, refer to the Applications Information section.

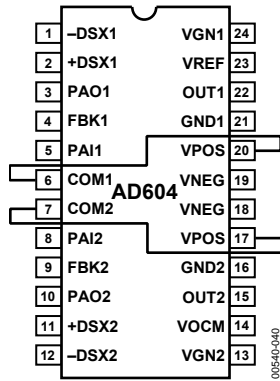


Figure 40. Shutdown of Preamplifiers Only

DIFFERENTIAL LADDER (ATTENUATOR)

The attenuator before the fixed gain amplifier of the DSX is realized by a differential 7-stage R-1.5R resistive ladder network with an untrimmed input resistance of 175Ω single-ended or 350Ω differential. The signal applied at the input of the ladder network (Figure 41) is attenuated by 6.908 dB per tap; thus, the attenuation at the first tap is 0 dB, at the second, 13.816 dB, and so on, all the way to the last tap where the attenuation is 48.356 dB.

A unique circuit technique is used to interpolate continuously between the tap points, thereby providing continuous attenuation from 0 dB to -48.36 dB . The ladder network, together with the interpolation mechanism, can be considered a voltage-controlled potentiometer.

Because the DSX circuit uses a single voltage power supply, the input biasing is provided by the VOCM buffer driving the the MID node (see Figure 41). Without internal biasing, the user would have to dc bias the inputs externally. If not done carefully, the biasing network can introduce additional noise and offsets. By providing internal biasing, the user is relieved of this task and only needs to ac couple the signal into the DSX. Note that the input to the DSX is still fully differential if driven differentially, that is, Pins +DSX and -DSX see the same signal but with opposite polarity (see the Ultralow Noise, Differential Input-Differential Output VGA section).

What changes is the load as seen by the driver; it is 175Ω when each input is driven single-ended, but 350Ω when driven differentially. This can be easily explained when thinking of the ladder network as just two 175Ω resistors connected back-to-back with the middle node, MID, being biased by the VOCM buffer. A differential signal applied between the +DSX and -DSX nodes results in zero current into the MID node, but a single-ended signal applied to either input, +DSX or -DSX, while the other input is ac grounded causes the current delivered by the source to flow into the VOCM buffer via the MID node.

The ladder resistor value of 175Ω provides the optimum balance between the load driving capability of the preamplifier and the noise contribution of the resistors. An advantage of the X-AMP architecture is that the output referred noise is constant vs. gain over most of the gain range. This is easily explained by looking at Figure 41 and observing that the tap resistance is equal for all taps after only a few taps away from the inputs. The resistance seen looking into each tap is 54.4Ω , which makes $0.95 \text{ nV}/\sqrt{\text{Hz}}$ of Johnson noise spectral density. Since there are two attenuators, the overall noise contribution of the ladder network is $\sqrt{2}$ times $0.95 \text{ nV}/\sqrt{\text{Hz}}$ or $1.34 \text{ nV}/\sqrt{\text{Hz}}$, a large fraction of the total DSX noise. The balance of the DSX circuit components contribute another $1.2 \text{ nV}/\sqrt{\text{Hz}}$, which together with the attenuator produces $1.8 \text{ nV}/\sqrt{\text{Hz}}$ of total DSX input referred noise.

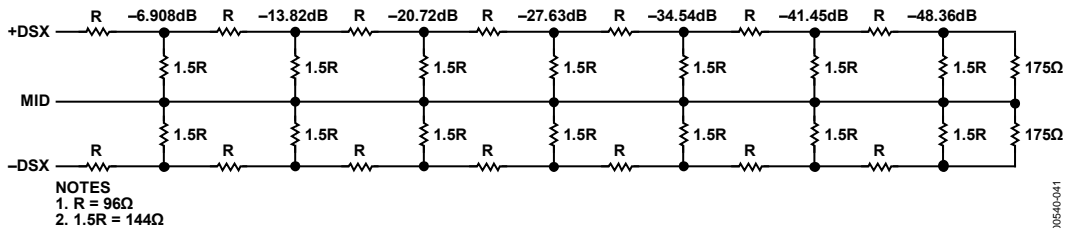


Figure 41. R-1.5R Dual Ladder Network

AC COUPLING

The DSX portion of the AD604 is a single-supply circuit and, therefore, its inputs need to be ac-coupled to accommodate ground-based signals. External capacitors C1 and C2 in Figure 37 level shift the ground referenced preamplifier output from ground to the dc value established by VO_{CM} (nominal 2.5 V). C1 and C2, together with the 175 Ω looking into each of the DSX inputs (+DSX and –DSX), act as high-pass filters with corner frequencies depending on the values chosen for C1 and C2. For example, if C1 and C2 are 0.1 μF, then together with the 175 Ω input resistance seen into each side of the differential ladder of the DSX, a –3 dB high-pass corner at 9.1 kHz is formed.

If the AD604 output needs to be ground referenced, another ac coupling capacitor is required for level shifting. This capacitor also eliminates any dc offsets contributed by the DSX. With a nominal load of 500 Ω and a 0.1 μF coupling capacitor, this adds a high-pass filter with –3 dB corner frequency at about 3.2 kHz.

The choice for all three of these coupling capacitors depends on the application. They should allow the signals of interest to pass unattenuated, while at the same time, they can be used to limit the low frequency noise in the system.

GAIN CONTROL INTERFACE

The gain control interface provides an input resistance of approximately 2 MΩ at Pin VGN1 and gain scaling factors from 20 dB/V to 40 dB/V for V_{REF} input voltages of 2.5 V to 1.25 V, respectively. The gain scales linearly-in-dB for the center 40 dB of gain range, which for VGN is equal to 0.4 V to 2.4 V for the 20 dB/V scale, and 0.2 V to 1.2 V for the 40 dB/V scale. Figure 42 shows the ideal gain curves for a nominal preamplifier gain of 14 dB, which are described by the following equations:

$$G (20 \text{ dB/V}) = 20 \times VGN - 5, VREF = 2.500 \text{ V} \quad (4)$$

$$G (20 \text{ dB/V}) = 30 \times VGN - 5, VREF = 1.666 \text{ V} \quad (5)$$

$$G (20 \text{ dB/V}) = 40 \times VGN - 5, VREF = 1.250 \text{ V} \quad (6)$$

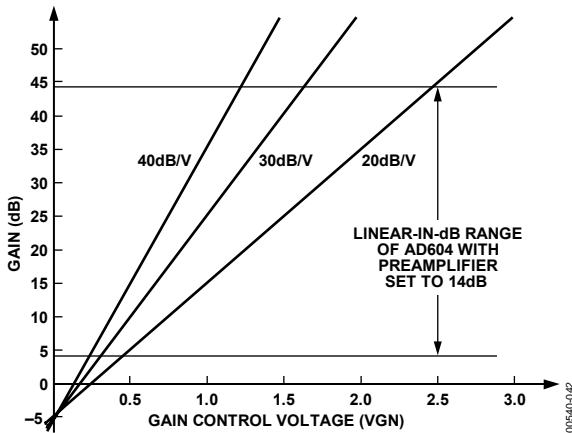


Figure 42. Ideal Gain Curves vs. VGN

From these equations, it can be seen that all gain curves intercept at the same –5 dB point; this intercept is +6 dB higher (+1 dB) if the preamplifier gain is set to +20 dB or +14 dB, lower (–19 dB) if the preamplifier is not used at all. Outside of the central linear range, the gain starts to deviate from the ideal control law but still provides another 8.4 dB of range. For a given gain scaling, V_{REF} can be calculated as shown in Equation 7:

$$VREF = \frac{2.500 \text{ V} \times 20 \text{ dB/V}}{\text{Gain Scale}} \quad (7)$$

Usable gain control voltage ranges are 0.1 V to 2.9 V for 20 dB/V scale and 0.1 V to 1.45 V for the 40 dB/V scale. VGN voltages of less than 0.1 V are not used for gain control since below 50 mV, the channel (preamp and DSX) is powered down. This can be used to conserve power and, at the same time, to gate off the signal. The supply current for a powered-down channel is 1.9 mA; the response time to power the device on or off is less than 1 μs.

ACTIVE FEEDBACK AMPLIFIER (FIXED GAIN AMP)

To achieve single-supply operation and a fully differential input to the DSX, an AFA is utilized. The AFA is basically an op amp with two g_m stages; one of the active stages is used in the feedback path (therefore the name), while the other is used as a differential input. Note that the differential input is an open-loop g_m stage that requires it to be highly linear over the expected input signal range. In this design, the g_m stage that senses the voltages on the attenuator is a distributed one; for example, there are as many g_m stages as there are taps on the ladder network. Only a few of them are on at any one time, depending on the gain-control voltage.

The AFA makes a differential input structure possible since one of its inputs (G1) is fully differential; this input is made up of a distributed g_m stage. The second input (G2) is used for feedback. The output of G1 is some function of the voltages sensed on the attenuator taps, which is applied to a high gain amplifier (A0). Because of negative feedback, the differential input to the high gain amplifier has to be zero; this in turn implies that the differential input voltage to G2 times g_{m2} (the transconductance of G2) has to be equal to the differential input voltage to G1 times g_{m1} (the transconductance of G1).

Therefore, the overall gain function of the AFA is

$$\frac{V_{OUT}}{V_{ATTEN}} = \frac{g_{m1}}{g_{m2}} \times \frac{R1 + R2}{R2} \quad (8)$$

where:

V_{OUT} is the output voltage.

V_{ATTEN} is the effective voltage sensed on the attenuator.

$$(R1+R2)/R2 = 42$$

$$g_{m1}/g_{m2} = 1.25$$

The overall gain is thus 52.5 (34.4 dB).

The AFA offers additional features:

1. The ability to invert the signal by switching the positive and negative input to the ladder network.
2. The possibility of using the DSX1 input as a second signal input.
3. Fully differential high impedance inputs when both preamplifiers are used with one DSX (the other DSX could still be used alone).
4. Independent control of the DSX common-mode voltage.

Under normal operating conditions, it is best to connect a decoupling capacitor to Pin VOVM, in which case the

common-mode voltage of the DSX is half the supply voltage; this allows for maximum signal swing. Nevertheless, the common-mode voltage can be shifted up or down by directly applying a voltage to VOVM. It can also be used as another signal input, the only limitation being the rather low slew rate of the VOVM buffer.

If the dc level of the output signal is not critical, another coupling capacitor is normally used at the output of the DSX; again this is done for level shifting and to eliminate any dc offsets contributed by the DSX (see the AC Coupling section).

APPLICATIONS INFORMATION

The most basic circuit in Figure 43 shows the connections for one channel of the AD604. The signal is applied at Pin 5. RGN is normally 0, in which case the preamplifier is set to a gain of 5 (14 dB). When Pin FBK1 is left open, the preamplifier is set to a gain of 10 (20 dB) and the gain range shifts up by 6 dB. The ac coupling capacitors before Pin $-DSX1$ and Pin $+DSX1$ should be selected according to the required lower cutoff frequency. In this example, the $0.1\ \mu\text{F}$ capacitors, together with the $175\ \Omega$ seen looking into each of the DSX input pins, provide a $-3\ \text{dB}$ high-pass corner of about 9.1 kHz. The upper cutoff frequency is determined by the bandwidth of the channel, which is 40 MHz. Note that the signal can be simply inverted by connecting the output of the preamplifier to Pin $-DSX1$ instead of $+DSX1$; this is due to the fully differential input of the DSX.

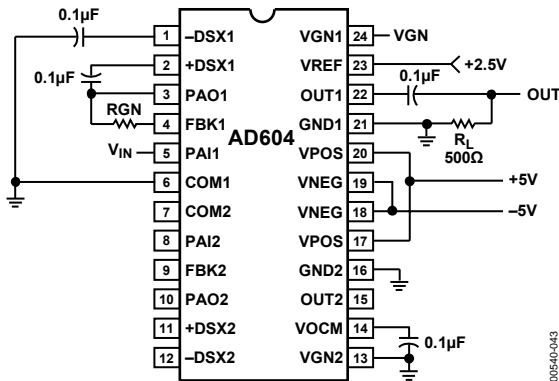


Figure 43. Basic Connections for a Single Channel

As shown here, the output is ac-coupled for optimum performance. In the case of connecting to the AD9050, ac coupling can be eliminated as long as Pin VOCM is biased by the same 3.3 V common-mode voltage as the AD9050 (see Figure 52).

Pin VREF requires a voltage of 1.25 V to 2.5 V, with between 40 dB/V and 20 dB/V gain scaling, respectively. Voltage VGN controls the gain; its nominal operating range is from 0.25 V to 2.65 V for 20 dB/V gain scaling and 0.125 V to 1.325 V for 40 dB/V scaling. When this pin is taken to ground, the channel powers down and disables its output.

Pin COM1 is the main signal ground for the preamplifier and needs to be connected with as short a connection as possible to the input ground. Since the internal feedback resistors of the preamplifier are very small for noise reasons ($8\ \Omega$ and $32\ \Omega$ nominally), it is of utmost importance to keep the resistance in this connection to a minimum. Furthermore, excessive inductance in this connection may lead to oscillations.

As a consequence of the ultralow noise and wide bandwidth of the AD604, large dynamic currents flow to and from the power supply. To ensure the stability of the part, extreme attention to supply decoupling is required. A large storage capacitor in parallel with a smaller high frequency capacitor connected right at the supply pins, together with a ferrite bead coming from the supply, should be used to ensure high frequency stability.

To provide for additional flexibility, Pin COM1 can be used to disable the preamplifier. When COM1 is connected to VP, the preamplifier is off, yet the DSX portion can be used independently. This may be of value when one desires to cascade the two DSX stages in the AD604. In this case, the first DSX output signal with respect to noise is large and using the second preamplifier at this point would waste power (see Figure 44).

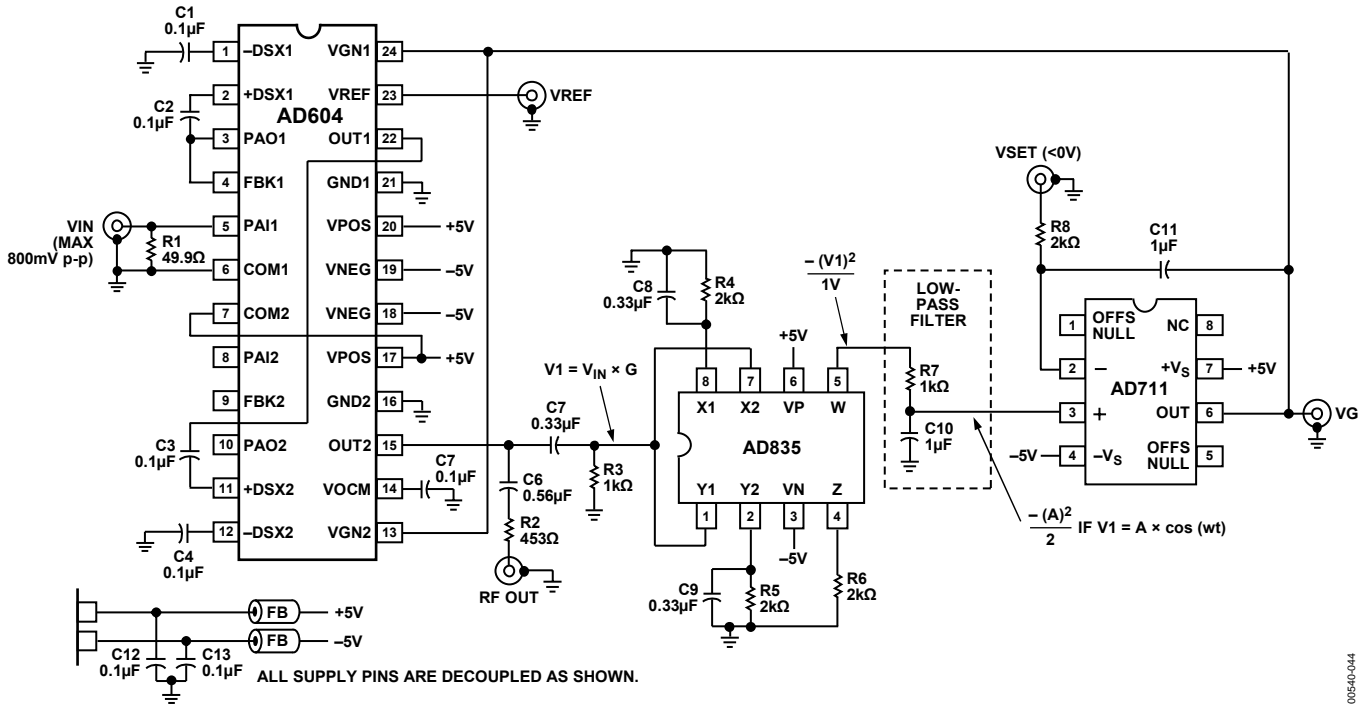


Figure 44. AGC Amplifier with 82 dB of Gain Range

AN ULTRALOW NOISE AGC AMPLIFIER WITH 82 dB TO 96 dB GAIN RANGE

Figure 44 shows an implementation of an AGC amplifier with 82 dB of gain range using a single AD604. First, the connections for the two channels of the AD604 are discussed; second, how the detector circuitry that closes the loop works is discussed.

The signal is applied to connector VIN, and since the signal source was 50 Ω, a terminating resistor (R1) of 49.9 Ω was added. The signal is then amplified by 14 dB (Pin FBK1 shorted to PAO1) through the Channel 1 preamplifier and is further processed by the Channel 1 DSX. Next, the signal is applied directly to the Channel 2 DSX. The second preamplifier is powered down by connecting its COM2 pin to the positive supply as explained in the Preamplifier section. Capacitor C1 and Capacitor C2 level shift the signal from the preamplifier into the first DSX and at the same time eliminate any offset contribution of the preamp. C3 and C4 have the same offset cancellation purpose for the second DSX. Each set of capacitors, together with the 175 Ω input resistance of the corresponding DSX, provides a high-pass filter with -3 dB corner frequency of about 9.1 kHz. Pin VOVM is decoupled to ground by a 0.1 μF capacitor, while VREF can be externally provided; in this application, the gain scale is set to 20 dB/V by applying 2.500 V. Since each of the DSX amplifiers operates from a single 5 V supply, the output is ac-coupled via C6 and C7. The output signal can be monitored at the connector labeled RF OUT.

Figure 45 and Figure 46 show the gain range and gain error for the AD604 connected as shown. The gain range is -14 dB to +82 dB; the useful range is 0 dB to +82 dB if the RF output amplitude is controlled to ±400 mV (+2 dBm). The main

limitation on the lower end of the signal range is the input capability of the preamplifier. This can be overcome by adding an attenuator in front of the preamplifier, but that would defeat the advantage of the ultralow noise preamplifier. It should be noted that the second preamplifier is not used since its ultralow noise and the associated high power consumption are overkill after the first DSX stage. It is disabled in this application by connecting the COM2 pin to the positive supply. Nevertheless, the second preamplifier can be used, if so desired, and the useful gain range increases by 14 dB to encompass 0 dB to 96 dB of gain. For the same +2 dBm output, this allows signals as small as -94 dBm to be measured.

To achieve the highest gains, the input signal must be band-limited to reduce the noise; this is especially true if the second preamplifier is used. If the maximum signal at Pin OUT2 of the AD604 is limited to ±400 mV (+2 dBm), the input signal level at the AGC threshold is +25 μV rms (-79 dBm). The circuit as shown has about 40 MHz of noise bandwidth; the 0.8 nV/√Hz of input referred voltage noise spectral density of the AD604 results in an rms noise of 5.05 μV in the 40 MHz bandwidth. The 50 Ω termination resistor, together with the 50 Ω source resistance of the signal generator, combine to an effective resistance as seen by the input of the preamplifier of 25 Ω, which makes 4.07 μV of rms noise in 40 MHz. The noise floor of this channel is consequently the rms sum of these two main noise sources, 6.5 μV rms. This means that the minimum detectable signal (MDS) for this circuit is +6.5 μV rms (-90.7 dBm). As a general rule, the measured signal should be about a factor of three larger than the noise floor, in this case 19.5 μV rms. Note that the 25 μV rms signal that this AGC circuit can correct for is just slightly above the MDS. Of course, the sensitivity of the

input can be improved by bandlimiting the signal; if the noise bandwidth is reduced by a factor of four to 10 MHz, the noise floor of the AGC circuit with a 50 Ω termination resistor drops to +3.25 μV rms (−96.7 dBm). Further noise improvement can be achieved by an input matching network or by transformer coupling of the input signal.

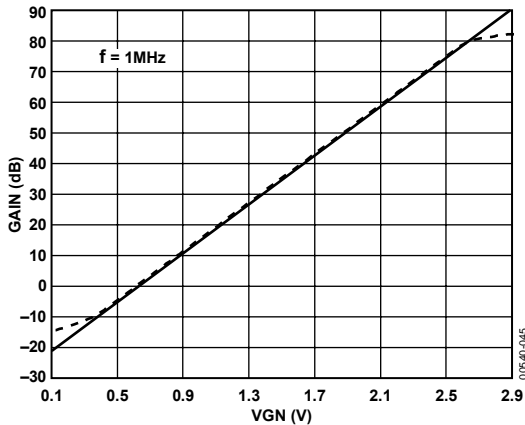


Figure 45. AD604 Cascaded Gain vs. VGN

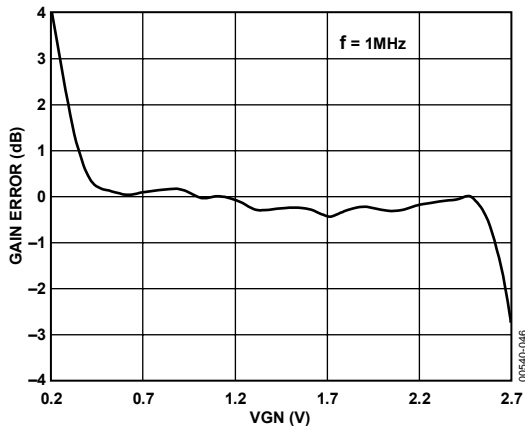


Figure 46. AD604 Cascaded Gain Error vs. VGN

The descriptions of the detector circuitry functions, comprised of a squarer, a low-pass filter, and an integrator, follow. At this point, it is necessary to make some assumptions about the input signal. The following explanation of the detector circuitry presumes an amplitude modulated RF carrier where the modulating signal is at a much lower frequency than the RF signal. The AD835 multiplier functions as the detector by squaring the output signal presented to it by the AD604. A low-pass filter following the squaring operation removes the RF signal component at twice the incoming signal frequency, while passing the low frequency AM information. The following integrator with a time constant of 2 ms set by R8 and C11 integrates the error signal presented by the low-pass filter and changes VG until the error signal is equal to V_{SET} .

For example, if the signal presented to the detector is $V1 = A \times \cos(\omega t)$ as indicated in Figure 44, the output of the squarer is $-(V1)^2/1$ V. The reason for all the minus signs in the detection circuitry comes from the necessity of providing negative feedback in the control loop; actually, if V_{SET} becomes greater

than 0 V, the control loop provides positive feedback. Squaring $A \times \cos(\omega t)$ results in two terms, one at dc and one at 2ω ; the following low-pass filter passes only the $-(A)^2/2$ dc term. This dc voltage is now forced equal to the voltage, V_{SET} , by the control loop. The squarer, together with the low-pass filter, functions as a mean-square detector. As should be evident by controlling the value of V_{SET} , the amplitude of the voltage V1 can be set at the input of the AD835; if V_{SET} equals -80 mV, the AGC output signal amplitude will be ± 400 mV.

Figure 47 shows the control voltage, VGN, vs. the input power at frequencies of 1 MHz (solid line) and 10 MHz (dashed line) at an output regulated level of 2 dBm (800 mV p-p). The AGC threshold is evident at a P_{IN} of about -79 dBm; the highest input power that could still be accommodated was about $+3$ dBm. At this level, the output starts being distorted because of clipping in the preamplifier.

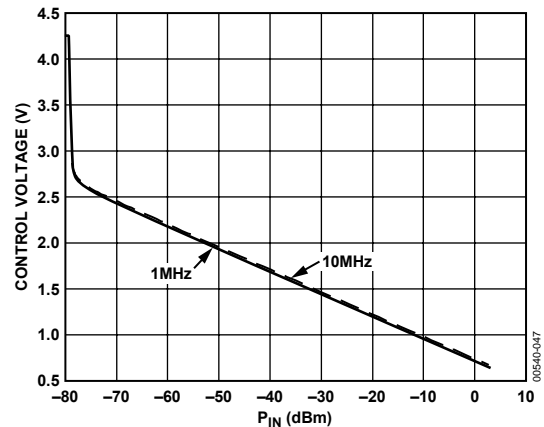


Figure 47. Control Voltage vs. Input Power of Circuit in Figure 44

As previously mentioned, the second preamplifier can be used to extend the range of the AGC circuit in Figure 44. Figure 48 shows the modifications that must be made to Figure 46 to achieve 96 dB of gain and dynamic range. Because of the extremely high gain, the bandwidth must be limited to reject some of the noise. Furthermore, limiting the bandwidth helps suppress high frequency oscillations. The added components act as a low-pass filter and dc block (C5 decouples the 2.5 V common-mode output of the first DSX). The ferrite bead has an impedance of about 5 Ω at 1 MHz, 30 Ω at 10 MHz, and 70 Ω at 100 MHz. The bead, combined with R2 and C6, forms a 1 MHz low-pass filter. At 1 MHz the attenuation is about -0.2 dB, increasing to -6 dB at 10 MHz and -28 dB at 100 MHz. Signals less than approximately 1 MHz are not significantly affected.

Figure 49 shows the control voltage vs. the input power at 1 MHz to the circuit in Figure 48; note that the AGC threshold is at -95 dBm. The output signal level was set to 800 mV p-p by applying -80 mV to the V_{SET} connector.

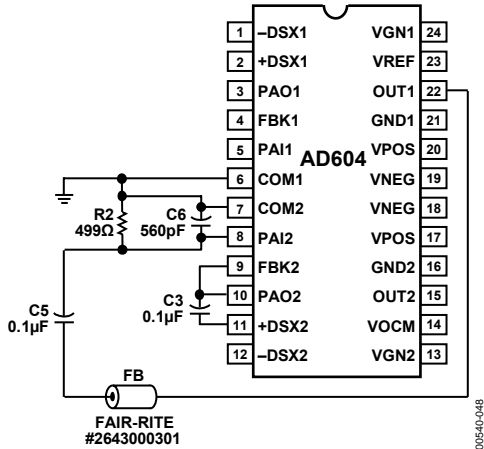


Figure 48. Modifications of AGC Amplifier to Create 96 dB of Gain Range

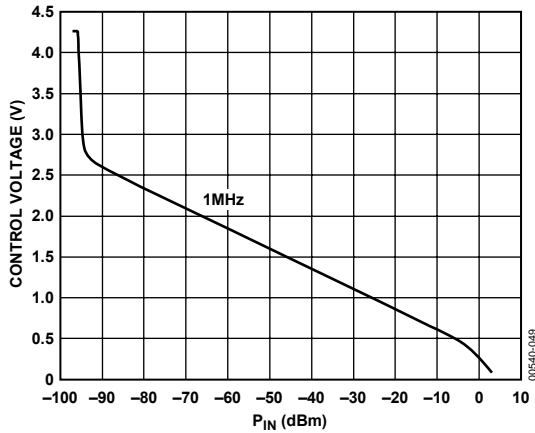


Figure 49. Control Voltage vs. Input Power of Circuit in Figure 48

ULTRALOW NOISE, DIFFERENTIAL INPUT-DIFFERENTIAL OUTPUT VGA

Figure 50 shows how to use both preamplifiers and DSXs to create a high impedance, differential input-differential output variable gain amplifier. This application takes advantage of the differential inputs to the DSXs. Note that the input is not truly differential, in the sense that the common-mode voltage needs to be at ground to achieve maximum input signal swing. This has largely to do with the limited output swing capability of the output drivers of the preamplifiers; they clip around ± 2.2 V due to having to drive an effective load of about 30Ω . If a different input common-mode voltage needs to be accommodated, ac coupling (as was done in Figure 48) is recommended. The differential gain range of this circuit runs from 6 dB to 54 dB. This is 6 dB higher than each individual channel of the AD604 because the DSX inputs now see twice the signal amplitude compared to when they are driven single-ended.

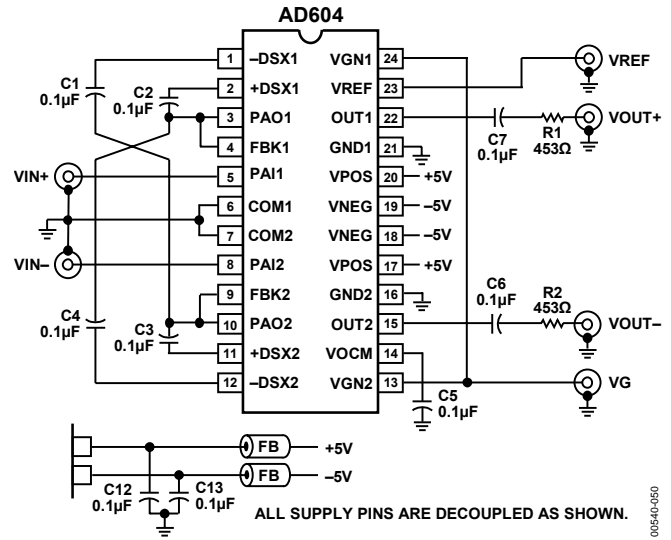
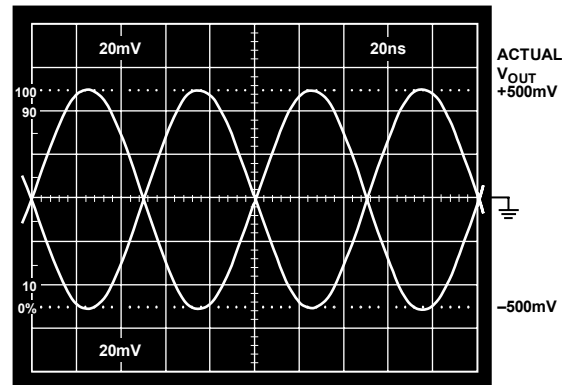


Figure 50. Ultralow Noise, Differential Input-Differential Output VGA

Figure 51 displays the output signals V_{OUT+} and V_{OUT-} after a -20 dB attenuator formed between the 453Ω resistors shown in Figure 50 and the 50Ω loads presented by the oscilloscope plug-in. $R1$ and $R2$ were inserted to ensure a nominal load of 500Ω at each output. The differential gain of the circuit was set to 20 dB by applying a control voltage, V_{GN} , of 1 V; the gain scaling was 20 dB/V for a V_{REF} of 2.500 V; the input frequency was 10 MHz and the differential input amplitude 100 mV p-p. The resulting differential output amplitude was 1 V p-p as can be seen on the scope photo when reading the vertical scale as 200 mV/div.



NOTES
1. THE OUTPUT AFTER $10\times$ ATTENUATOR FORMED BY 453Ω TOGETHER WITH 50Ω OF 7A24 PLUG-IN.

Figure 51. Output of VGA in Figure 50 for $V_{GN} = 1$ V

AD604

MEDICAL ULTRASOUND TGC DRIVING THE AD9050, A 10-BIT, 40 MSPS ADC

The AD604 is an ideal candidate for the time gain control (TGC) amplifier that is required in medical ultrasound systems to limit the dynamic range of the signal that is presented to the ADC. Figure 52 shows a schematic of an AD604 driving an AD9050 in a typical medical ultrasound application.

The gain is controlled by means of a digital byte that is input to an AD7226 DAC that outputs the analog gain control signal.

The output common-mode voltage of the AD604 is set to $V_{POS}/2$ by means of an internal voltage divider. The V_{OCM} pin is bypassed with a $0.1 \mu\text{F}$ capacitor to ground.

The DSX output is optionally filtered and then buffered by an AD9631 op amp, a low distortion, low noise amplifier. The op amp output is ac-coupled into the self-biasing input of an AD9050 ADC that is capable of outputting 10 bits at a 40 MSPS sampling rate.

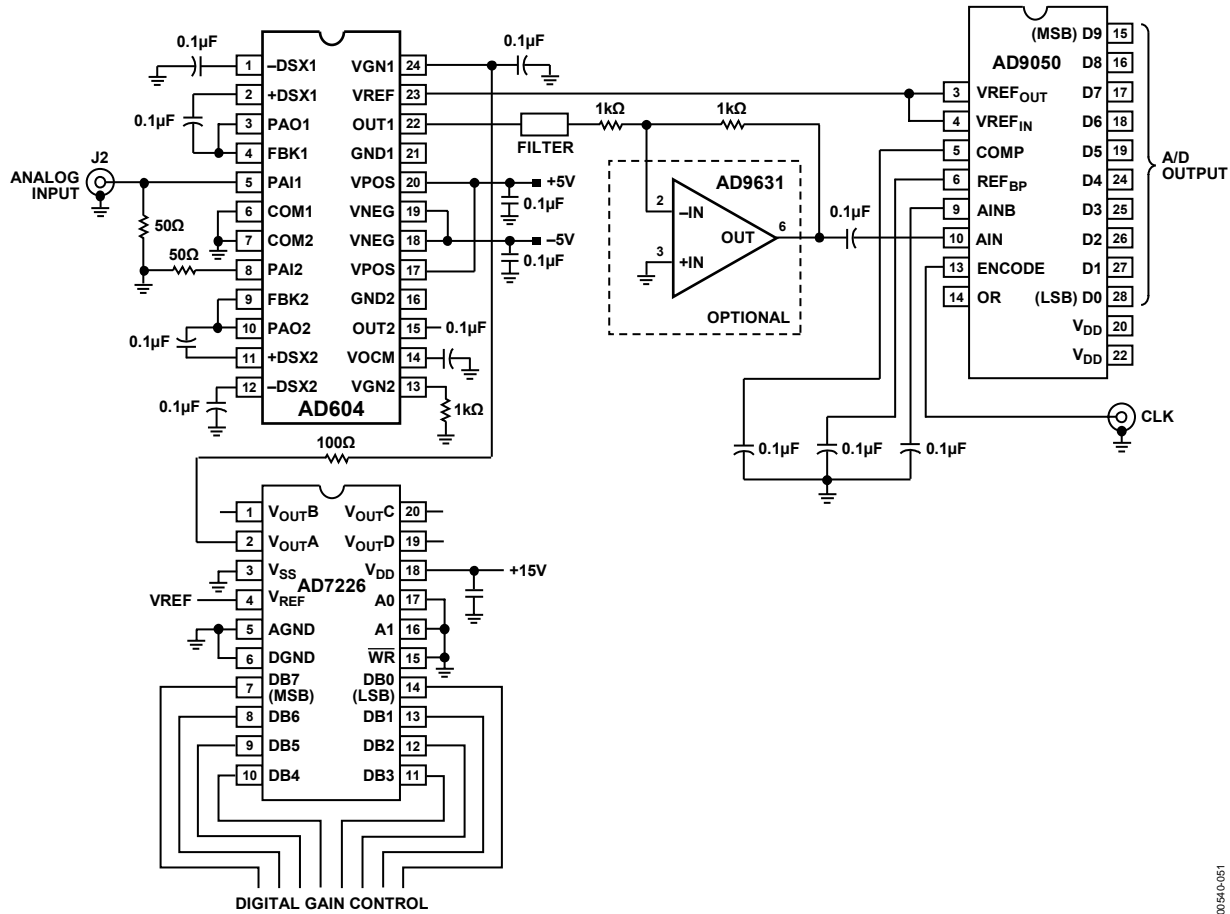
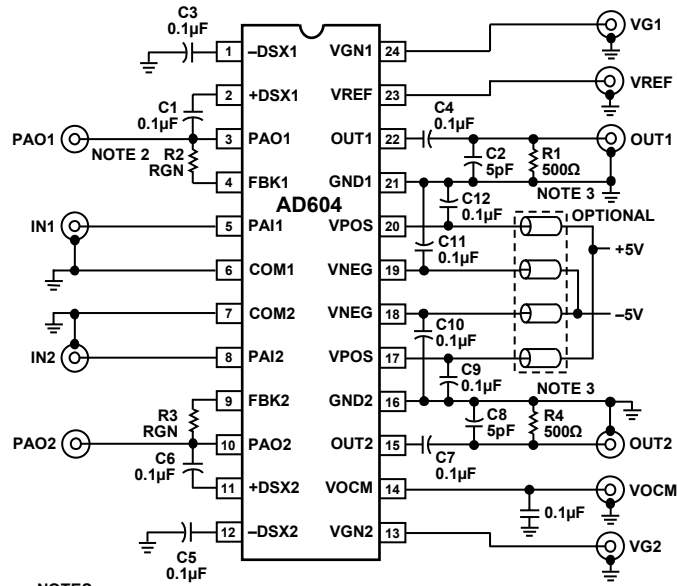


Figure 52. TGC Circuit for Medical Ultrasound Application

00540-051



- NOTES**
1. PAO1 AND PAO2 ARE USED TO MEASURE PREAMPS.
 2. RGN = 0 NOMINALLY; PREAMP GAIN = 5, RGN = OPEN; PREAMP GAIN = 10.
 3. WHEN MEASURING BW WITH 50Ω SPECTRUM ANALYZER, USE 450Ω IN SERIES.

Figure 53. Basic Test Board

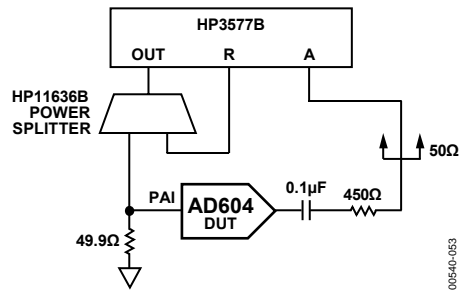


Figure 54. Setup for Gain Measurements

EVALUATION BOARD

Figure 55 is a photograph of the AD604-EVAL evaluation board assembly. Multiple input connections, test points, jumper selectable options, and on-board trims offer convenience when configuring the AD604 in various operating modes.

The evaluation board requires only a dual 5 V supply capable of 200 mA or higher to operate both channels. Prior to shipment, the evaluation board is fully tested. Users need only attach power supply leads and the appropriate test equipment to the board.

Because of this flexibility, not all component positions on the board are populated when the board is shipped. Installing or changing additional parts is optional.

The AD604-EVAL is fabricated on a four-layer board with inner power and ground layers. The AD604 is a stable, trouble-free device, however, as with all high frequency integrated circuits, power and ground planes help to ensure consistency in performance.

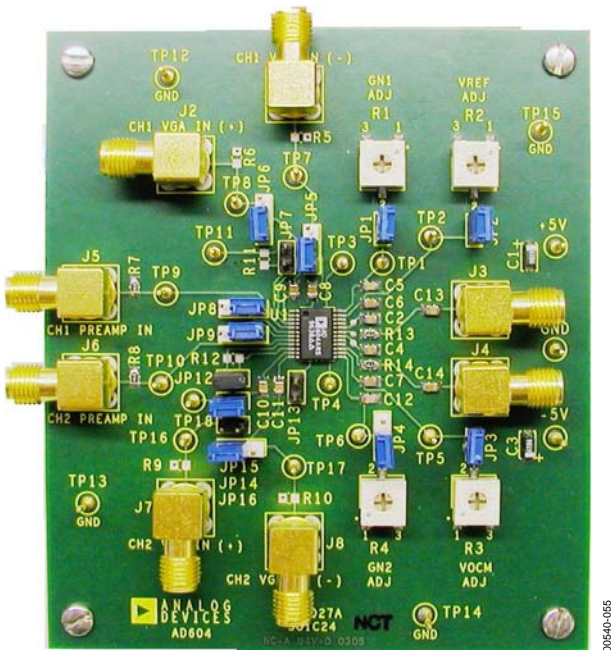


Figure 55. AD604-EVAL Assembly

USING THE PREAMP

To use the preamps, simply connect a signal source to CH1 PREAMP IN and/or CH2 PREAMP IN via the SMA connectors. Referring to the schematic in Figure 61, the input lines are terminated with 50 Ω resistors at locations R7 and R8.

To enable the preamps, insert jumpers in the JP 8 and JP 9 right most locations; this connects COM1 and COM2 to ground. Power down the preamps by inserting jumpers in the JP8 and JP9 left most positions.

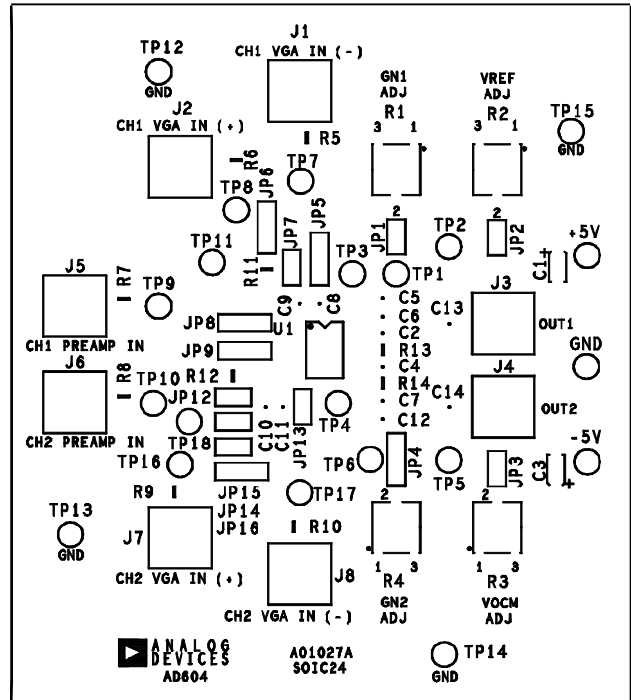


Figure 56. AD604 Evaluation Board—Component Side Silk Screen

DSX INPUT CONNECTIONS

The DSX inputs can be connected in single-ended or differential configurations. SMA connectors are provided for each of the inputs, and are labeled CH1, CH2, VGA IN (+) and VGA IN (-). Jumpers JP6 and JP15 select between the preamp outputs and the DSX inputs.

For direct drive of the Channel 1 VGA, insert a jumper in the top position of JP6. For direct drive of the Channel 2 VGA, insert a jumper in JP14 and verify that there are no jumpers in JP12 and JP13. Refer to the schematic shown in Figure 61 for circuit details.

Differential DSX Inputs

Differential inputs are possible using both polarities of the VGA SMA connectors and appropriate jumpers. Inserting a jumper in the lower position of JP5 selects the negative input of Channel 1. A jumper in the top position of JP6 selects the positive input of Channel 1. A jumper in JP16 right most position selects the negative input of Channel 2, and a jumper in JP14 selects the positive input. Again, verify there are no jumpers in JP15 or JP13.

Because the VGA section of the AD604 uses a single +5 V supply, the DSX inputs are ac coupled. Decoupling capacitors are provided on the evaluation board.

The DSX input impedance is approximately 200 Ω. Optional 66.5 Ω resistors can be installed across the inputs at positions R5, R6, R9, and R10 to establish a 50 Ω terminating load.

Connecting the DSX Inputs to the Preamps

To connect the DSX inputs to the preamps, install jumpers in the JP6 lower position and in JP15. Verify that the jumpers in JP13 and JP14 are removed.

Cascaded DSX

To channel cascade the two channels, insert a jumper in JP13. The resulting single channel gain range is 96 dB. Verify that jumpers JP14 and JP15 are removed.

The gains of cascaded VGAs may be controlled independently or in common. For common control, insert a jumper in the top position of JP4. To use the trimmer as a gain control, insert a jumper in JP1. For external control, remove JP 1 and connect a signal source at TP1 or TP6.

PREAMPLIFIER GAIN

Jumpers in JP 7 and JP 12 select between two preamplifier gains: 14 dB and 20 dB. Intermediate gains are derived by installing resistors in positions R 11 and R 12. The 14 dB and 20 dB preset gains are accurate due to close matching of thin

film resistors. The gain accuracy after installing external resistors is subject to inherent tolerance of absolute accuracy.

OUTPUTS

The DSX outputs are available on OUT1 and OUT2 SMA connectors and are series-terminated with decoupled 49.9 Ω and a series resistor. These components may be replaced to accommodate other output impedances.

DC OPERATING CONDITIONS

Table 4 lists the trimmers and their functions provided for convenient dc level adjustments of gain, reference voltage, and output common-mode voltage. Table 5 lists the jumpers and their functions.

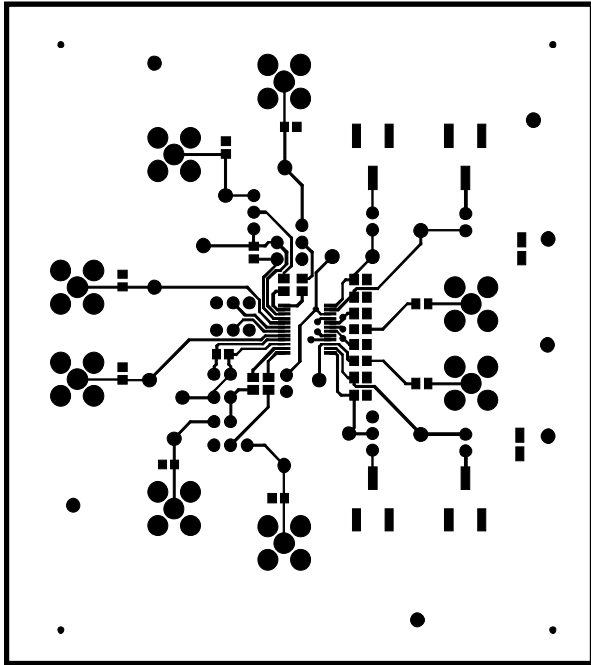
Table 4. Trimmer Functions

Trimmer	Function
R1	Gain of Channel 1
R2	Reference voltage adjustment
R3	Output common-mode voltage adjustment
R4	Channel 2 gain adjustment

Table 5. Jumpers

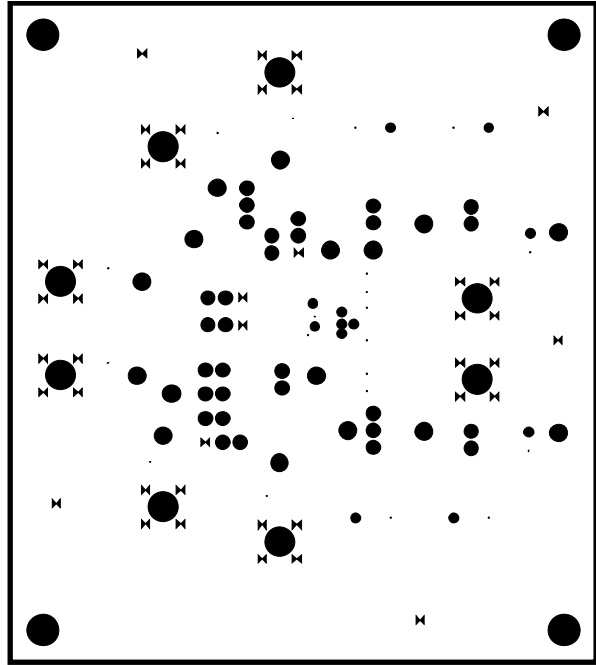
Jumper No.	Function
1	Connects R1 gain adjust wiper to Pin VGN1.
2	Connects R2 reference voltage trimmer to VREF input.
3	Connects common-mode voltage trimmer to VOCM Pin.
4	Connects Pin VGN2 to R4 Channel 2 gain trimmer or to Pin VGN1 or common gain adjustment.
5	Connects -DSX1 Pin to CH1 VGA IN (-) or to ground.
6	Connects +DSX1 (ac-coupled) to preamp output of Channel 1 or to the CH 1 VGA IN (+) SMA connector.
7	When open, the Preamp 1 Gain is 20 dB; Preamp Gain 1 is 14 dB when a shunt is installed.
8	Shunt in left position disables Preamp 1; shunt in right most position enables Preamp 1.
9	Shunt in left position disables Preamp 2; shunt in right most position enables Preamp 2.
12	When open, the Preamp 2 gain is 20 dB; Preamp 2 gain is 14 dB when a shunt is installed.
13	Cascades DSX2 with DSX 1 when a jumper is inserted.
14	Connects +DSX2 (ac-coupled) to preamp output of Channel 2 or to the CH 2 VGA IN (+) SMA connector.
15	Connects +DSX2 (ac-coupled) to preamp output of Channel 2.
16	Connects -DSX2 Pin to CH2 VGA IN (-) or to ground.

EVALUATION BOARD ARTWORK AND SCHEMATIC



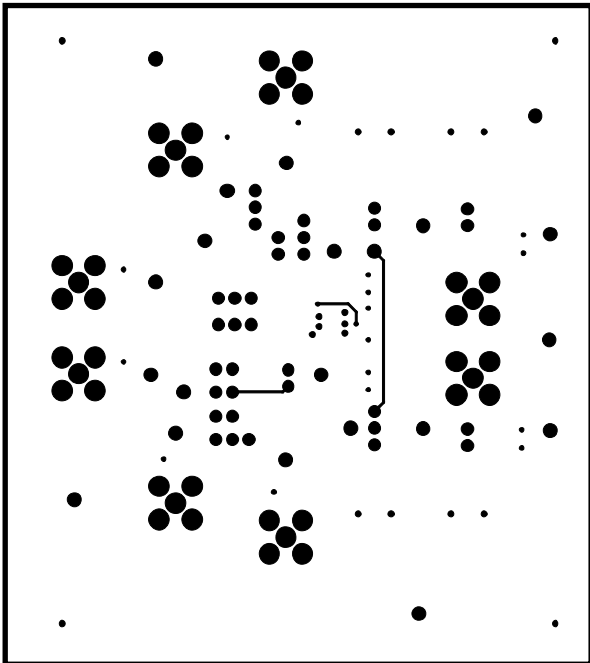
00540-057

Figure 57. Component Side Copper



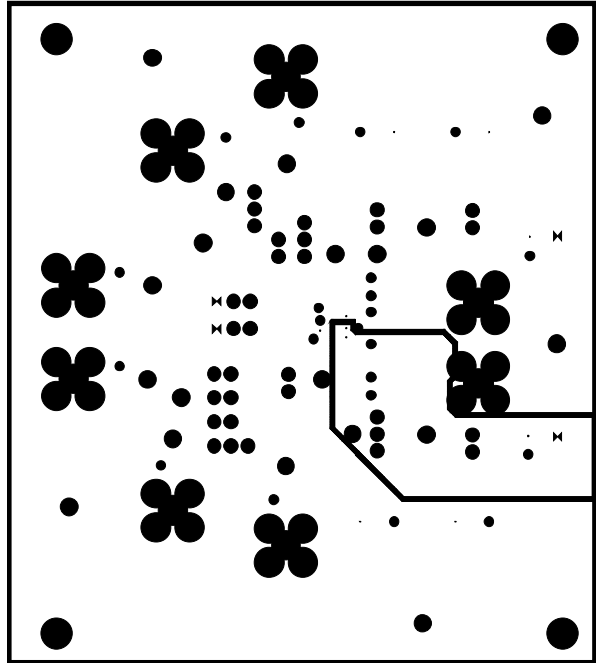
00540-059

Figure 59. Internal Ground Plane



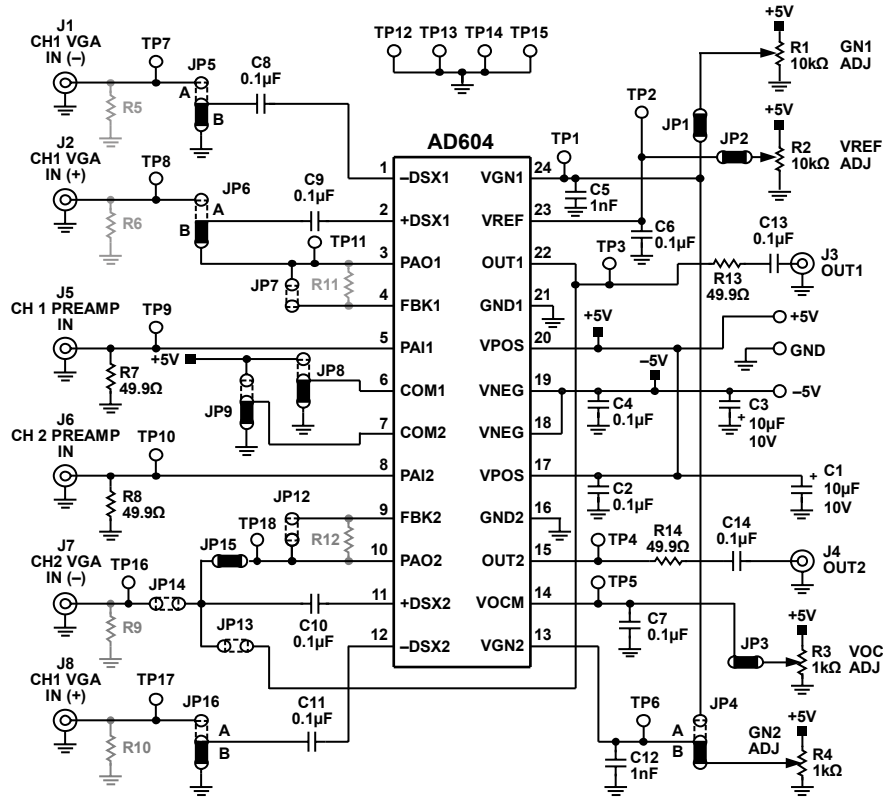
00540-058

Figure 58. Secondary Side Copper



00540-060

Figure 60. Internal Power Plane



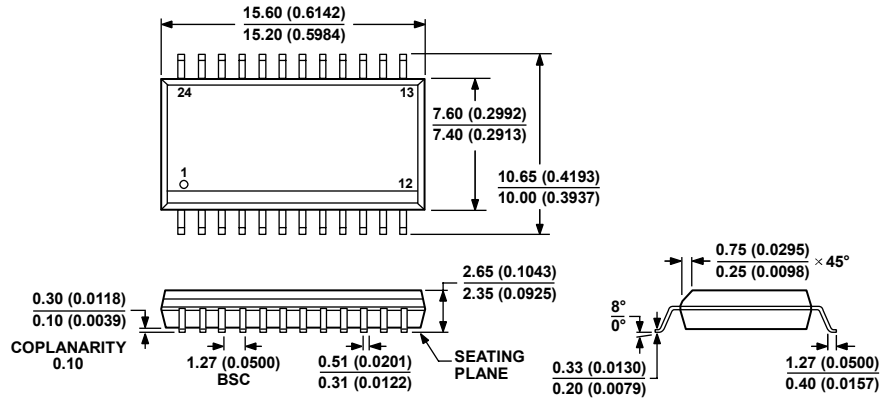
NOTES
1. PARTS IN GRAY ARE NOT INSTALLED.

Figure 61. Schematic

Table 6. Bill of Materials

Qty.	Name	Description	Reference Designator	Manufacturer	Part Number
1	Test Loop	Red	+5 V	Components Corp.	TP-104-01-02
1	Test Loop	Blue	-5 V	Components Corp.	TP-104-01-06
5	Test Loop	Black	GND, TP12, TP13, TP14, TP15	Components Corp.	TP-104-01-00
14	Test Loop	Purple	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP16, TP17, TP18	Components Corp.	TP-104-01-07
2	Capacitor	Tantalum 10 μ F 10 V A size	C1, C3	Nichicon	F931A106MAA
10	Capacitor	0.1 μ F 50 V 20% 0805	C2, C4, C6, C7, C8, C9, C10, C11, C13, C14	Panasonic	PCC1840CT-ND
2	Capacitor	SM 1000 pF 50 V 0805	C5, C12	Panasonic	ECU-V1H102KBN
8	Connector	SMA FEM PC MOUNT, RA	J1, J2, J3, J4, J5, J6, J7, J8	Amphenol	901-143-6RFX
8	Header	0.1" center 2-pin	JP1, JP2, JP3, JP7, JP12, JP13, JP14, JP15	Berg	69157-2
6	Header	0.1" center 3-pin	JP4, JP5, JP6, JP8, JP9, JP16	Molex	22-11-2032
4	Trimmer	10 k Ω 1/4" SM	R1, R2, R3, R4	Bourns	3361P-1-103G
4	Resistor	49.9 Ω 1% 1/10 W 0805	R7, R8, R13, R14	Panasonic	ERJ-6ENF49.9
1	Integrated Circuit	40 MHz. Dual Low Noise VGA	U1 (AD604)	Analog Devices, Inc.	AD604AR
10	Jumper	Mini Jumper	Install in headers at JP1, JP2, JP3, JP4 lower, JP5 lower, JP6 lower, JP8 right, JP9 right, JP15, JP16 left		

OUTLINE DIMENSIONS

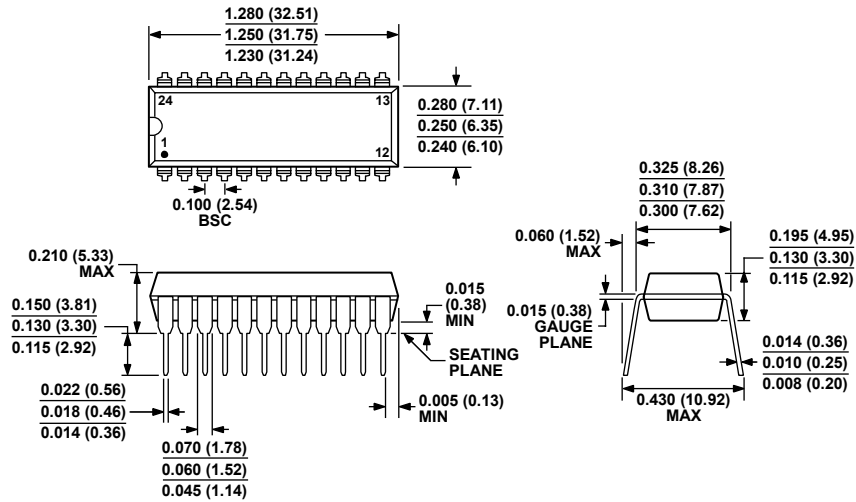


COMPLIANT TO JEDEC STANDARDS MS-013-AD
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 62. 24-Lead Standard Small Outline Package [SOIC_W]
 Wide Body
 (RW-24)

Dimensions shown in millimeters and (inches)

060706-A

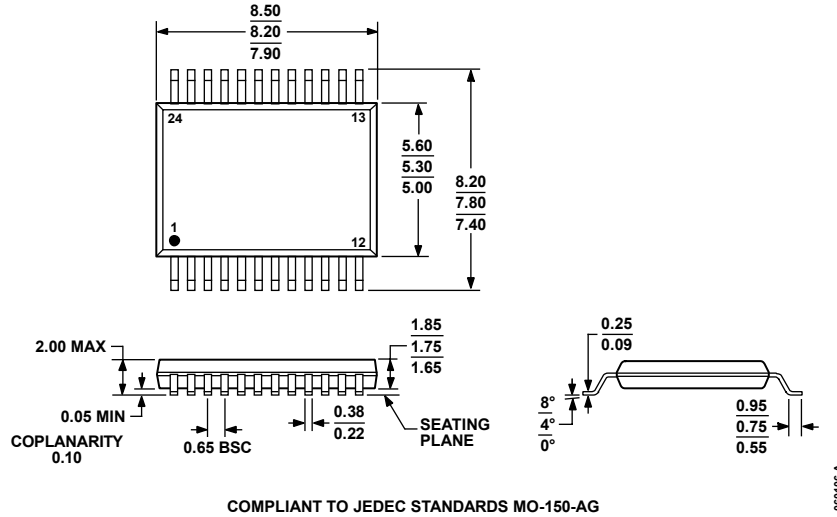


COMPLIANT TO JEDEC STANDARDS MS-001
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
 CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 63. 24-Lead Plastic Dual In-Line Package [PDIP]
 Narrow Body
 (N-24-1)

Dimensions shown in inches and (millimeters)

071006-A



COMPLIANT TO JEDEC STANDARDS MO-150-AG
 Figure 64. 24-Lead Shrink Small Outline Package [SSOP]
 (RS-24)
 Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD604AN	-40°C to +85°C	24-Lead Plastic Dual In-Line Package [PDIP]	N-24-1
AD604ANZ ¹	-40°C to +85°C	24-Lead Plastic Dual In-Line Package [PDIP]	N-24-1
AD604AR	-40°C to +85°C	24-Lead Standard Small Outline Package [SOIC_W]	RW-24
AD604AR-REEL	-40°C to +85°C	24-Lead Standard Small Outline Package [SOIC_W]	RW-24
AD604ARZ ¹	-40°C to +85°C	24-Lead Standard Small Outline Package [SOIC_W]	RW-24
AD604ARZ-RL ¹	-40°C to +85°C	24-Lead Standard Small Outline Package [SOIC_W]	RW-24
AD604ARS	-40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP]	RS-24
AD604ARS-REEL	-40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP]	RS-24
AD604ARS-REEL7	-40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP]	RS-24
AD604ARSZ ¹	-40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP]	RS-24
AD604ARSZ-RL ¹	-40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP]	RS-24
AD604ARSZ-RL7 ¹	-40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP]	RS-24
AD604-EVAL		Evaluation Board	

¹ Z = RoHS Compliant Part.

AD604

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AD604

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